MVME2502

Installation and Use

P/N: 6806800R96B

April 2014

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About this Manual

Overview of Contents

This manual is divided into the following chapters and appendices.

- *Introduction* gives an overview of the features of the product, standard compliances, mechanical data, and ordering information.
- *Hardware Preparation and Installation* outlines the installation requirements, hardware accessories, switch settings, and installation procedures.
- *Controls, LEDs, and Connectors* describes external interfaces of the board. This includes connectors and LEDs.
- *Functional Description* includes a block diagram and functional description of major components of the product.
- *Memory Maps and Registers* contains information on system resources including system control and status registers and external timers.
- *Boot System* describes the boot loader software.
- *Programming Model* contains additional programming information for the board.
- *Replacing the Battery* contains the procedures for replacing the battery.
- *Related Documentation* provides a listing of related product documentation, manufacturer's documents, and industry standard specifications.
- *Safety Notes* summarizes the safety instructions in the manual.
- *Sicherheitshinweise* is a German translation of the Safety Notes chapter.

Abbreviations

This document uses the following abbreviations:

Term	Definition
CPLD	Complex Programmable Logic Device
DDR	Double Data Rate
DDR3	Double Data Rate 3
DMI	Direct Media Interface

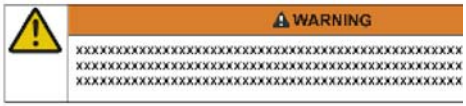
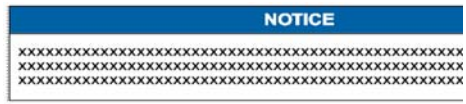
Term	Definition
DUART	Dual UART
EEPROM	Erasable Programmable Read-Only Memory
FCC	Federal Communications Commission
GB	GigaByte
Gbit	Gigabit
Gbps	Gigabits per second
HDD	Hard Disk Drive
I/O	Input/Output
IEEE	Institute of Electrical and Electronics Engineers
LED	Light Emitting Diode
MHz	Megahertz
MCP	Multi-Chip Package
MRAM	Magnetoresistive Random Access Memory
OS	Operating System
PCB	Printed Circuit Board
PCI	Peripheral Component Interconnect
PCI-E	PCI Express
PCI-X	Peripheral Component Interconnect eXtended
PIM	PCI Mezzanine Card Input/Output Module
PLD	Programmable Logic Device
PMC	PCI Mezzanine Card (IEEE P1386.1)
PrPMC	Processor PCI Mezzanine Card
RTC	Real-Time Clock
RTM	Rear Transition Module
SATA	Serial Advanced Technology Attachment
UART	Universal Asynchronous Receiver-Transmitter

Term	Definition
USB	Universal Serial Bus
VITA	VMEbus International Trade Association
VME	Versa Module Eurocard
XMC	PCI Express Mezzanine Card

Conventions

The following table describes the conventions used throughout this manual.

Notation	Description
0x00000000	Typical notation for hexadecimal numbers (digits are 0 through F), for example used for addresses and offsets
0b0000	Same for binary numbers (digits are 0 and 1)
bold	Used to emphasize a word
`Screen`	Used for on-screen output and code-related elements or commands in body text
`Courier + Bold`	Used to characterize user input and to separate it from system output
Reference	Used for references and for table and figure descriptions
File > Exit	Notation for selecting a submenu
<text>	Notation for variables and keys
[text]	Notation for software buttons to click on the screen and parameter description
...	Repeated item for example node 1, node 2, ..., node 12
. . .	Omission of information from example/command that is not necessary at the time being
..	Ranges, for example: 0..4 means one of the integers 0,1,2,3, and 4 (used in registers)

Notation	Description
|	Logical OR
	Indicates a hazardous situation which, if not avoided, could result in death or serious injury
	Indicates a hazardous situation which, if not avoided, may result in minor or moderate injury
	Indicates a property damage message
	No danger encountered. Pay attention to important information

Summary of Changes

This manual has been revised and replaces all prior editions.

Part Number	Publication Date	Description
6806800R96A	October 2013	Initial Version
6806800R96B	April 2014	Re-branded to Artesyn template. Added *MVME2502 Declaration of Conformity on page 22*. Added Flash Memory Map and updated SPI Flash Memory, Reset Switch and PMC/XMC Sites. Added *Installation of MVME2502HDMNKIT1 and MVME2502-HDMNKIT2*.

1.1 Overview

The MVME2502 is a VME form-factor single-board based on the Freescale QorlQ P2020 (dual-core) processor. It has a 6U form-factor and has an expansion slot for two PCI Mezzanine Card (PMC) or PCI express Mezzanine Card (XMC). It comes with 2 GB of DDR3 SDRAM, and is offered with either IEEE 1101.10 compliant or SCANBE ejector handles.

The front panel I/O configuration consists of two RJ45 10/100/1000BASE-T Ethernet ports, a USB 2.0 port, a Micro DB9 RS-232 serial console port, and a reset/abort switch. It also has an LED to signal board failure and another LED that can be configured in the LED register.

The rear I/O includes support for VMEbus (Legacy VME, VME 64, VME64x, and 2eSST), rear PMC/XMC I/O, RTM I/O (through VME P2), two 10/100/1000BASE-T Ethernet, four UART, and RTM I2C/Presence/Power. See the table below for a summary of the features of the MVME2502.

Table 1-1 Key Features of the MVME2502

Function	Features
Processor	• Freescale QorIQ P2020 (dual-core) • 1000 MHz to 1.2 GHzcore frequency • 512 KB L2 cache • Three 10/100/1000 Mbps enhanced three-speed Ethernet controllers (eTSECs) • Two PCI-E 1.0a x1 interface controller • One PCI-E 1.0a x2 interface controller • USB 2.0 interface • Enhanced secure digital host controller • DDR3 memory controller at 800 MT/s • SPI interface (four chip selects, but only two are used on the board) • Enhanced local bus controller • UART • Two I2C interfaces • Programmable interrupt controller
Memory	2 GB DDR3-800 soldered chip memory with ECC

Table 1-1 Key Features of the MVME2502 (continued)

Function	Features
Front panel I/O	● Micro DB9 RS-232 serial console port ● USB 2.0 ● Two RJ45 10/100/1000BASE-T Ethernet ● Reset/Abort switch ● Fail LED and User LED ● PMC/XMC front panel I/O (optional)
Backplane I/O	● VME Bus ● RTM I/O (through VME P2) ● PMC/XMC I/O with P4 I/O ● Two 10/100/1000BASE-T Ethernet ● Four UART ● RTM I2C/Presence/Power
Expansion	Expansion site 1: ● PMC supporting PCI-X 64/33 interface ● XMC supporting PCI-E 1.0a x2 interface Expansion site 2: ● SATA drive kit
Boot Flash	16 MB SPI Flash
Persistent Data Storage	512 KB MRAM
User Flash	8GB eMMC soldered down
I2C Devices	● Real-Time Clock ● Board Temperature Sensor ● 8 KB VPD EEPROM ● Two 64 KB User EEPROM
CPLD	Watchdog, timers, and registers
Boot Firmware	U-Boot-based firmware image in 16 MB SPI Flash. This flash is split into two 8 MB chips.

Table 1-1 Key Features of the MVME2502 (continued)

Function	Features
Operating System	• Based from BSP provided by Freescale which is based from standard Linux version 2.6.32-rc3 • Development tool is ltib 9.1.1 (Linux Target Image Builder) from Freescale • VxWorks

1.2 Standard Compliances

The product is designed to meet the following standards. Results are pending until testing is finished.

Table 1-2 Board Standard Compliances

Standard	Description
EN 60950-1/A11:2009 IEC 60950-1:2005 2nd Edition CAN/CSA C22.2 No 60950-1	Safety Requirements (legal)
FCC Part 15, Subpart B, Class A (non-residential) ICES-003, Class A (non-residential) EMC Directive 89/336/EEC EN55022 Class B EN55024 AS/NZS CISPR 22, Class A EN300386	EMC requirements (legal) on system level (predefined Artesyn system)
ETSI EN 300 019 series	Environmental Requirements
Directive 2011/65/EU	Directive on the restriction of the use of certain hazardous substances in electrical and electronic equipment (RoHS)

Figure 1-1 MVME2502 Declaration of Conformity

EC Declaration of Conformity

According to EN 17050-1:2004

Manufacturer's Name:	Artesyn Embedded Technologies
Manufacturer's Address:	Zhongshan General Carton Box Factory Co. Ltd. No 62, Qi Guan Road West, Shiqi District, 528400 Zhongshan City Guangdong, PRC

Declares that the following product, in accordance with the requirements of 2004/108/EC, 2006/95/EC, 2011/65/EU and their amending directives,

Product:	MVME2502 Series Single-Board Computers
Model Name/Number:	MVME2502-02100202E, MVME2502-02100202S, MVME2502-02120201E, MVME2502-02120201E, MVME2502-021CC

has been designed and manufactured to the following specifications:

EN55022:2006 Class A

EN55024: (A1: 2001 + A2: 2003): 1998

2011/65/EU RoHS Directive

As manufacturer we hereby declare that the product named above has been designed to comply with the relevant sections of the above referenced specifications. This product complies with the essential health and safety requirements of the above specified directives. We have an internal production control system that ensures compliance between the manufactured products and the technical documentation.

Tom Tuttle, Manager, Product Testing Services

03/11/2014
Date (MM/DD/YYYY)

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1.3 Mechanical Data

The following table provides details about the dimensions and weight of the board.

Table 1-3 Mechanical Data

Feature	Value
Height	233.44 mm (9.2 inches)
Depth	160.0 mm (6.3 inches)
Front Panel Height	261.8 mm (10.3 inches)
Width	19.8 mm (0.8 inches)
Max. Component Height	14.8 mm (0.58 inches)
Weight	400 grams (ENP1), 700 grams (ENP2)

1.4 Ordering Information

As of the printing date of this manual, this guide supports the models listed below.

Table 1-4 Accessories and Cables

Order Number	Description
MVME2502-02100202E	QorIQ P2020 1.0GHz, 2GB DDR3 2PMC/XMC ENP2 EXTENDED TEMP, IEEE
MVME2502-02100202S	QorIQ P2020 1.0GHz, 2GB DDR3 2PMC/XMC ENP2 EXTENDED TEMP, SCANBE
MVME2502-02120201E	QorIQ P2020 1.2GHz, 2GB DDR3 2PMC/XMC ENP1 IEEE
MVME2502-02120201S	QorIQ P2020 1.2GHz, 2GB DDR3 2PMC/XMC ENP1 SCANBE
MVME2502-021CC	QorIQ P2020 1.0GHz, 2GB DDR3 2PMC/XMC ENP2 EXT TEMP, IEEE

As of the printing date of this manual, the following board accessories are available.

Table 1-5 Accessories and Cables

Order Number	Description
SERIAL-MINI-D2	SERIAL CABLE - MICRO D SUB CONNECTOR TO STANDARD DB9
ACC/CABLE/SER/DTE/6E	SERIAL CABLE, RD 009, 2M, 2 DTE MD/D, RJ45 TO DB9
MVME2502-HDMNTKIT1	MVME2502 HD MOUNTING KIT ENP1
MVME2502-HDMNTKIT2	MVME2502 HD MOUNTING KIT ENP2

1.5 Product Identification

The following graphics shows the location of the serial number label.

Figure 1-2 Serial Number Location-ENP1 Variant

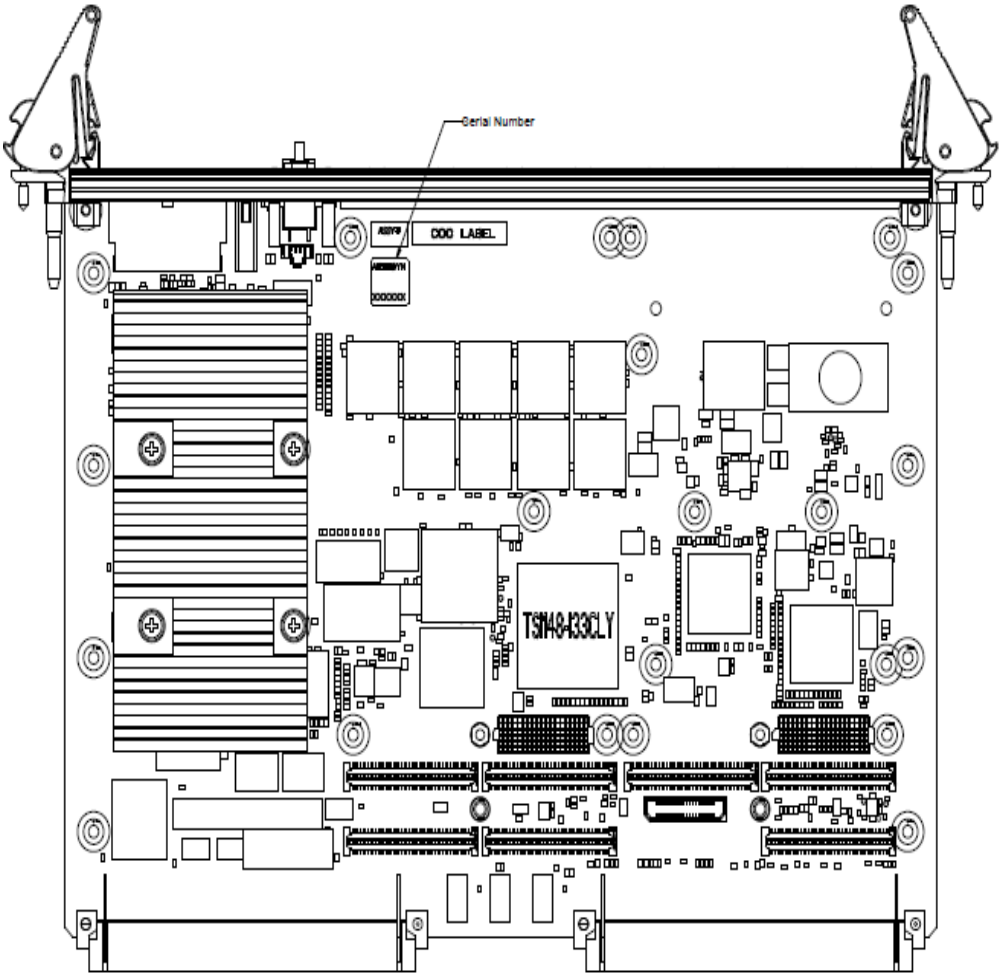
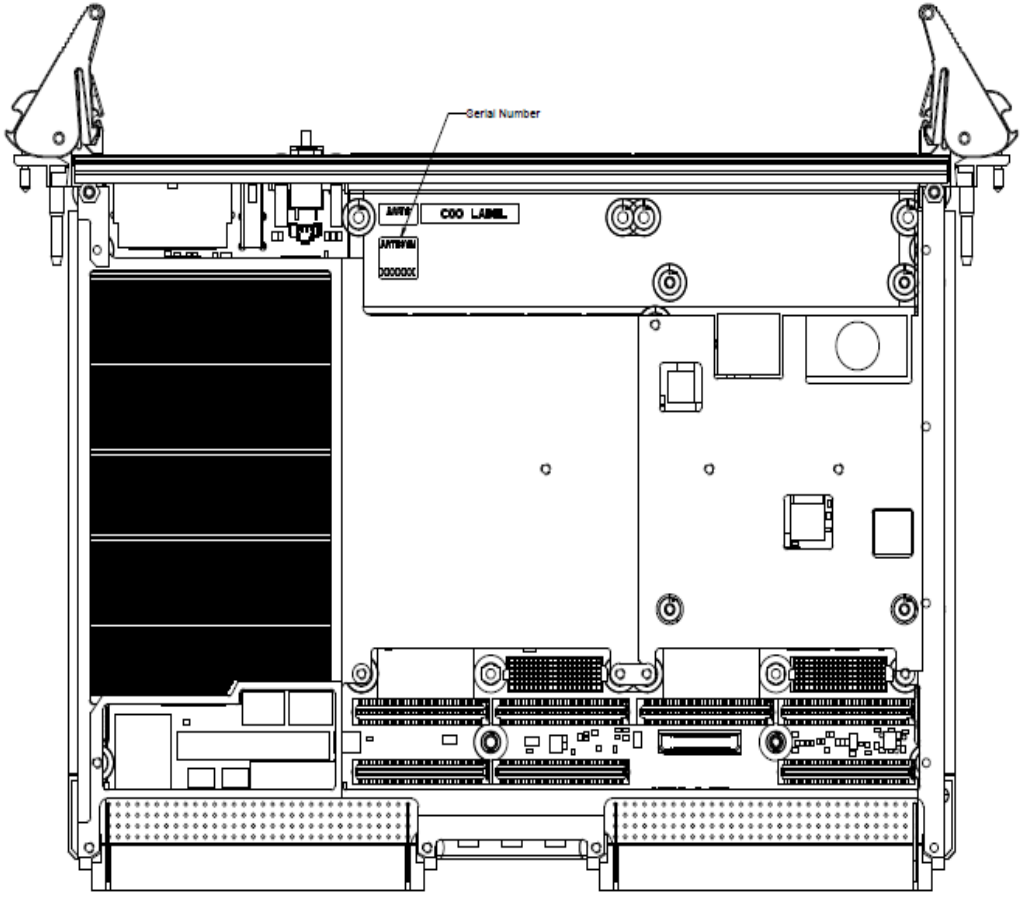


Figure 1-3 Serial Number Location-ENP2 Variant



Chapter 2

Hardware Preparation and Installation

2.1 Overview

This chapter provides installation and safety instructions for this product. Installation instructions for the optional PMC and transition module are also included.

A fully implemented MVME2502 consists of the base board plus:

- PCI Mezzanine Card (PMC) or PCI-E Mezzanine Card (XMC) for added versatility
- Rear transition module
- SATA kit

NOTE: MVME2502-HDMNKIT1/MVME2502-HDMNKIT2 is provided based on purchase order.

The following are the things that need to be done before using the board. Be sure to read the entire chapter, including all caution and warning notes, before you begin.

1. Unpack the hardware. Refer to *Unpacking and Inspecting the Board* on page 28
2. Configure the hardware by setting jumpers on the board and RTM. Refer to *Configuring the Board* on page 31
3. Install the transition module in the chassis. Refer to *Rear Transition Module* on page 32.
4. Install PMC module (if required). Refer to *PMC/XMC Support* on page 33.
5. Install XMC span module (if required). Refer to *PMC/XMC Support* on page 33.
6. If purchased, install MVME2502-HDMNKIT1/MVME2502-HDMNKIT2. Refer to *Installation of MVME2502-HDMNTKIT1/MVME2502-HDMNTKIT2* on page 35.
7. Install the board in the chassis. Refer to *Installing and Removing the Board* on page 37.
8. Attach cables and apply power. Refer to *Completing the Installation* on page 39.

2.2 Unpacking and Inspecting the Board

Read all notices and cautions prior to unpacking the product.

NOTICE

- Damage of Circuits
  Electrostatic discharge and incorrect installation and removal can damage circuits or shorten its life.
- Before touching the board or electronic components, make sure that you are working in an ESD-safe environment.

Shipment Inspection

1. Verify that you have received all items of your shipment.
2. Check for damage and report any damage or differences to customer service.
3. Remove the desiccant bag shipped together with the board and dispose of it according to your country's legislation.

The product is thoroughly inspected before shipment. If any damage occurred during transportation or any items are missing, contact customer service immediately.

2.3 Requirements

Make sure the board meets the requirements specified in the next sections when the board is operated in your particular system configuration.

2.3.1 Environmental Requirements

Operating temperatures refer to the temperature of the air circulating around the board and not to the component temperature.

Table 2-1 Environmental Requirements

Characteristics	Commercial Versions	Extended Temperature Versions
Applicable Variants	MVME2502-02120201E/S MVME2502-02120202E/S	MVME2502-02100202E MVME2502-02100202S
Cooling Method	Forced Air	Forced Air
Operating Temperature	0°C to +55°C	-40°C to +71°C
Storage	-40°C to +85°C	-50°C to +100°C
Vibration Sine (10min/axis)	2 G, 5 to 500 Hz	5 G, 15 to 2000 Hz
Vibration Random (1hr/axis)	0.002g2/Hz, 15 to 2000 Hz	0.04g2/Hz, 15 to 2000 Hz (8 GRMS)[2]
Shock	20g/11 mS	30g/11 mS
Humidity	to 95% RH (non-condensing)	to 100% RH (non-condensing)

1. ft3/min

2. Flat 15-1000Hz, -6db/octave 1000Hz - 2000Hz [MIL-STD 810F Figure 514.5C-17]

NOTICE

Product Damage

- High humidity and condensation on the board surface causes short circuits.
- Do not operate the board outside the specified environmental limits.
- Make sure the board is completely dry and there is no moisture on any surface before applying power.

2.3.2 Power Requirements

The board uses +5.0 V from the VMEbus backplane. On board power supply generates the required voltages for the various ICs. The MVME2502 connects the +12 V and -12 V supplies from the backplane to the PMC sites, while the +3.3 V power supplied to the PMC sites comes from the +5.0 V backplane power. A maximum of 10 A of +3.3 V power is available to the PMC sites, however the 90 W +5.0 V limit must be observed as well as any cooling limitations.

The following table provides an estimate of the typical and maximum power required.

Table 2-2 Power Requirements

Board Variant	Maximum (Calculated)	Typical (Measured Operating)
MVME2502-02120201E	28.93W	21.8
MVME2502-02120201S	28.93W	21.8
MVME2502-02100202E	23.33W	16.6
MVME2502-02100202S	23.33W	16.6

The power is measured when the board is in standby (Linux prompt). Power will significantly increase when adding hard drives or a XMC/PMC card.

The following table shows the power available when the MVME2502 is installed in either a three row or five row chassis and when PMCs are present.

Chassis Type	Available Power	Power With PMCs
Three Row	70 W maximum	below 70 W
Five Row	90 W maximum	below 90 W

Keep below power limit. Cooling limitations must be considered.

2.3.3 Equipment Requirements

The following are recommended to complete a MVME2502 system:

- VMEbus system enclosure
- System console terminal
- Operating system (and/or application software)
- Transition module and connecting cables

2.4 Configuring the Board

The board provides software control over most options. Settings can be modified to fit the user's specifications. To configure, set the bits in the control register after installing the board in a system. Make sure that all user-defined switches are properly set before installing a PMC/XMC module. For more information, see *Switches* on page 64.

2.5 Installing Accessories

2.5.1 Rear Transition Module

The MVME2502 does not support hot swap. Remove power to the rear slot or system before installing the module. A PCMI/O Module (PIM) needs to be manually configured and installed before placing the transition module.

NOTICE

Damage of Circuits

- Electrostatic discharge and incorrect installation and removal can damage circuits or shorten its life.
- Before touching the board or electronic components, make sure that you are working in an ESD-safe environment.

Product Damage

- Only use injector handles for board insertion to avoid damage to the front panel and/or PCB. Deformation of the front panel can cause an electrical short or other board malfunction.

Board Malfunction

- Switches marked as “reserved” might carry production-related functions and can cause the board to malfunction if their setting is changed.
- Do not change settings of switches marked as “reserved”. The setting of switches which are not marked as “reserved” has to be checked and changed before board installation.

Installation and Removal Procedure

1. Turn OFF all equipment and disconnect the power cable from the AC power source.
2. Remove the chassis cover.
3. Remove the filler panel(s) from the appropriate card slot(s) at the rear of the chassis (if the chassis has a rear card cage).

4. Install the top and bottom edge of the transition module into the rear guides of the chassis.
5. Ensure that the levers of the two injector/ejectors are in the outward position.
6. Slide the transition module into the chassis until resistance is felt.
7. Move the injector/ejector levers in an inward direction.
8. Verify that the transition module is properly seated and secure it to the chassis using the two screws adjacent to the injector/ejector levers.
9. Connect the cables to the transition module.

To remove the transition module from the chassis, reverse the procedure and press the red locking tabs (IEEE handles only) to extract the board.

2.5.2 PMC/XMC Support

Installation Procedure

Read all notices and follow these steps to install a PMC on the baseboard.

NOTICE

Damage of Circuits

- Electrostatic discharge and incorrect installation and removal can damage circuits or shorten its life.
- Before touching the board or electronic components, make sure that you are working in an ESD-safe environment.

Product Damage

- Inserting or removing modules with power applied may result in damage to module components.
- Before installing or removing additional devices or modules, read the documentation that came with the product.

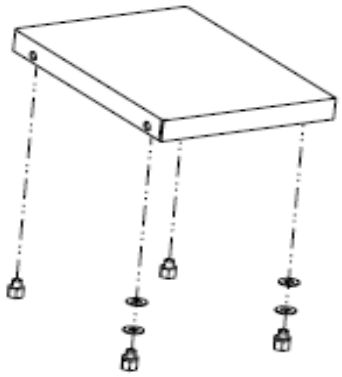
1. Attach an ESD strap to your wrist. Attach the other end of the strap to the chassis as a ground. Make sure that it is securely fastened throughout the procedure.
2. Remove the PMC/XMC filler plate from the front panel cut-out.
3. Slide the front bezel of the PMC/XMC into the cut-out from behind. The front bezel of the PMC/XMC module will be flushed with the board when the connectors on the module align with the mating connectors on the board.
4. Align the mating connectors properly and apply minimal pressure to the PMC/XMC until it is seated to the board.
5. Insert the four PMC/XMC mounting screws through the mounting holes on the bottom side of the board, and then thread the four mount points on the PMC/XMC. Tighten the screws.
6. Install the board into the appropriate card slot. Make sure that the board is well seated into the backplane connectors. Do not damage or bend connector pins.
7. Replace the chassis or system cover.
8. Reconnect the system to the power source and then turn on the system.

When removing the PMC/XMC, hold it by its long side and exert minimal force when pulling it from the baseboard to prevent pin damage.

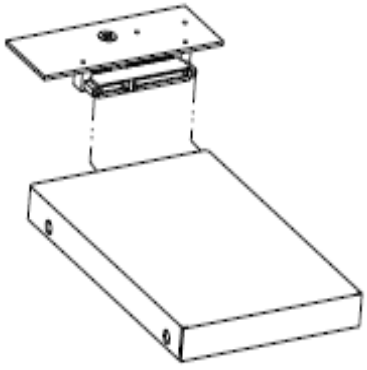
2.5.3 Installation of MVME2502-HDMNTKIT1/MVME2502-HDMNTKIT2

Installation Procedure

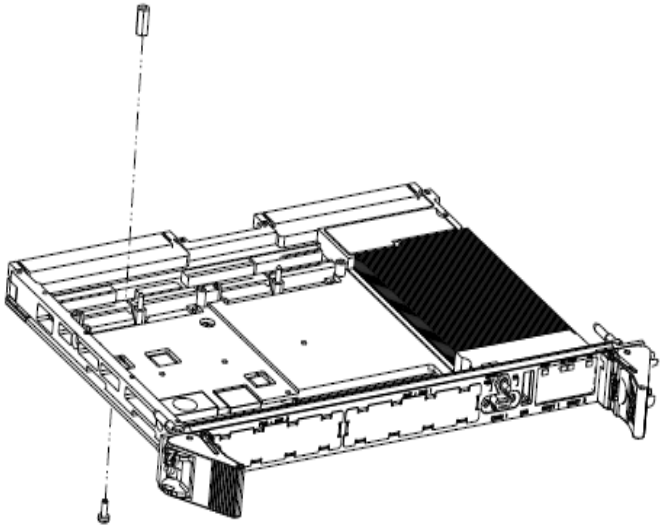
1. Attach washers and hex standoffs to HDD received with the MVME2502-HDMNTKIT1 / MVME2502-HDMNTKIT2.



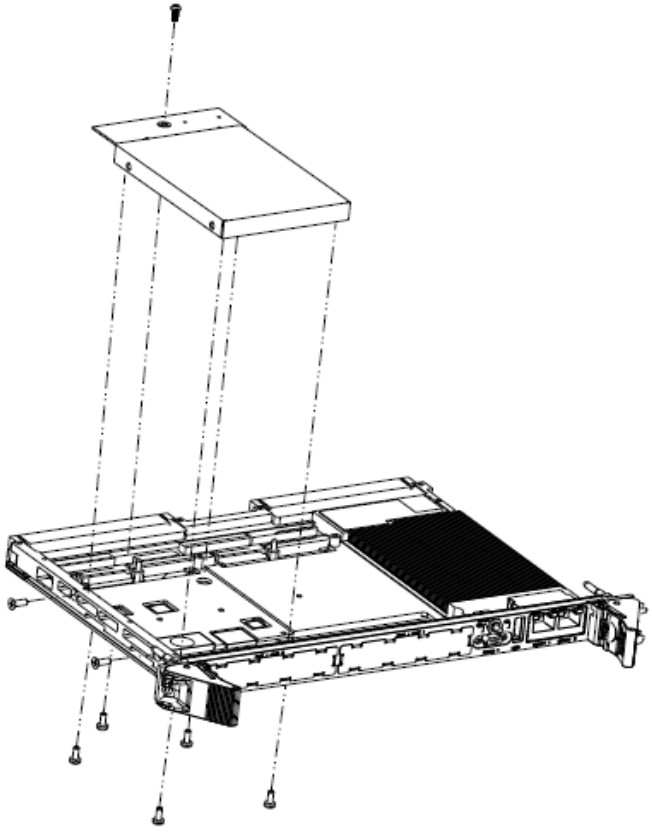
2. Mate the SATA adapter board to the blade, making sure that it is properly aligned with the standoff. Use the screws to anchor the SATA adapter board to the blade.



3. Attach hex standoff to main board.



4. Attach HDD with interface PCB to main board using screws as shown below:



2.6 Installing and Removing the Board

This section describes the recommended procedure for installing the board in a chassis. Read all warnings and instructions before installing the board.

The MVME2502 does not support hot swap. Power off the slot or system and make sure that the serial ports and switches are properly configured.

NOTICE

Damage of Circuits

- Electrostatic discharge and incorrect installation and removal can damage circuits or shorten its life.
- Before touching the board or electronic components, make sure that you are working in an ESD-safe environment.

Product Damage

- Only use injector handles for board insertion to avoid damage to the front panel and/or PCB. Deformation of the front panel can cause an electrical short or other board malfunction.

1. Attach an ESD strap to your wrist. Attach the other end of the strap to an electrical ground. Make sure that it is securely fastened throughout the procedure.
2. Remove VME filler panels from the VME enclosures, as appropriate.
3. Install the top and bottom edge of the board into the guides of the chassis.
4. Ensure that the levers of the two injector/ejectors are in the outward position.
5. Slide the board into the chassis until resistance is felt.
6. Simultaneously move the injector/ejector levers in an inward direction.
7. Verify that the board is properly seated and secure it to the chassis using the two screws located adjacent to the injector/ejector levers.
8. Connect the appropriate cables to the board.

To remove the board from the chassis, reverse the procedure and press the red locking tabs (IEEE handles only) to extract the board.

2.7 Completing the Installation

The board is designed to operate as an application-specific computer blade or an intelligent I/O board/carrier. It can be used in any slot in a VME chassis. Once the board is installed, you are ready to connect peripherals and apply power to the board.

NOTICE

Product Damage

- RJ-45 connectors on modules are either twisted-pair Ethernet (TPE) or E1/T1/J1 network interfaces. Connecting an E1/T1/J1 line to an Ethernet connector may damage your system.
- Make sure that TPE connectors near your working area are clearly marked as network connectors.
- Verify that the length of an electric cable connected to a TPE bushing does not exceed 100 meters.
- Make sure the TPE bushing of the system is connected only to safety extra low voltage circuits (SELV circuits).
- If in doubt, ask your system administrator.

The console settings for the MVME2502 are:

- Eight bits per character
- One stop bit per character
- Parity disabled (no parity)
- Baud rate of 9600 baud

Verify that hardware is installed and the power/peripheral cables connected are appropriate for your system configuration.

Replace the chassis or system cover, reconnect the chassis to power source, and turn the equipment power on.

3.1 Board Layout

The following figure shows the components and connectors on the MVME2502.

Figure 3-1 Board Layout ENP1 Variant

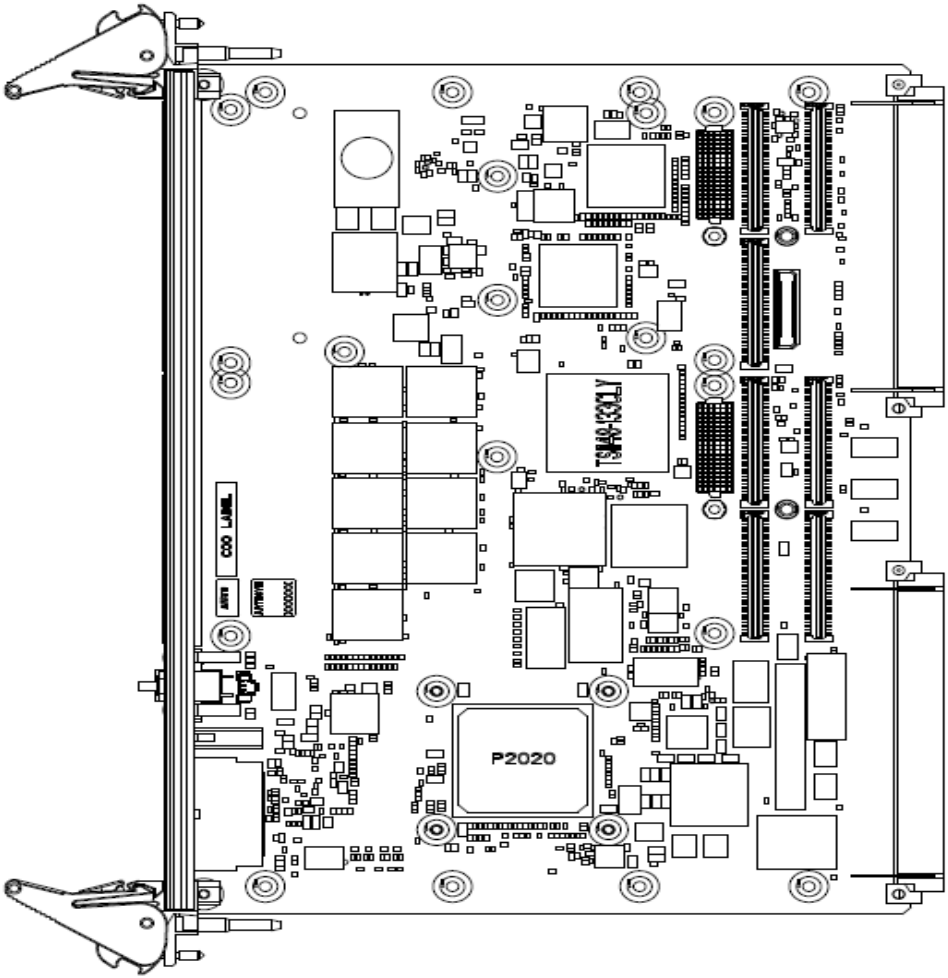
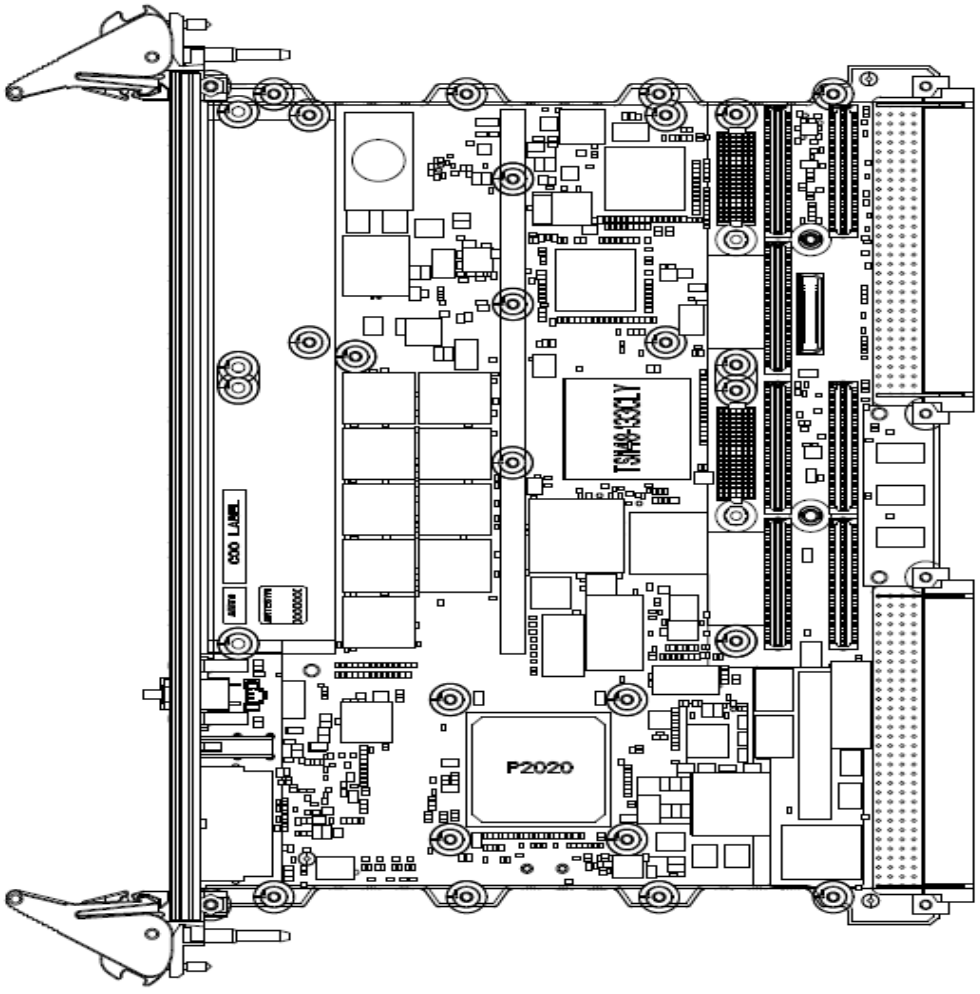


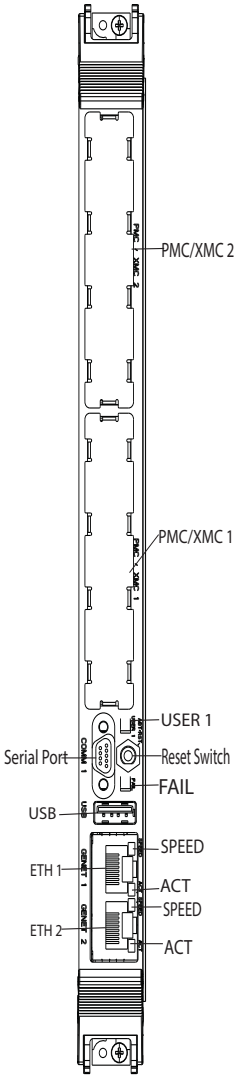
Figure 3-2 Board Layout ENP2 Variant



3.2 Front Panel

The following components are found on the MVME2502 ENP1 and ENP2 front panel.

Figure 3-3 Front Panel LEDs, Connectors and Switches



3.2.1 Reset Switch

The MVME2502 has a single push button switch that has both the abort and reset functions. Pressing the switch for less than three seconds can generate an abort interrupt if there is firmware that will read the GPIO2 (0xffdf0095) interrupt register. U-boot does not implement any interrupts and also does not detect the interrupt or display anything when the button is pressed.

Holding it down for more than three seconds will generate a hard reset. The VME SYSRESET is generated if the MVME2502 is the VMEbus system controller.

3.3 LEDs

The MVME2502 utilizes light emitting diodes (LEDs) to provide a visible status indicator on the front panel. These LEDs show power failures, power up states, Ethernet link/speed, Ethernet activity, SATA link and activity and PCIe valid lane status. There are also a few user configurable LEDs. Each LED description is necessary for troubleshooting and debugging.

3.3.1 Front Panel LEDs

The front panel LEDs are listed below

Figure 3-4 Front Panel LEDs

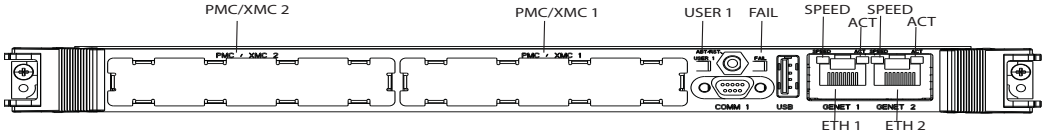


Table 3-1 Front Panel LEDs

Label	Function	Location	Color	Description
USER 1	User Defined	Front panel	Off Yellow Red	By default User Software Controllable. Refer to the "User LED Register." User Software Controllable. Refer to the "User LED Register."

Table 3-1 Front Panel LEDs (continued)

Label	Function	Location	Color	Description
FAIL	Board Fail	Front panel	Off Red	Normal operation after successful firmware boot. One or more on-board power rails has failed and the board has shutdown to protect the hardware. Normal during power up, during hardware reset (such as a front panel reset). May be asserted by the BDFAIL bit in the Tsi148 VSTAT register.
GENET1 SPEED	TSEC1 Link/Speed	Front panel Integrated RJ45 LED	Off Amber Green	No link 10/100BASE-T operation 1000 BASE-T operation
GENET1 ACT	TSEC1 Activity	Front panel Integrated RJ45 LED	Off Blinking Green	No activity Activity proportional to bandwidth utilization
GENET2 SPEED	TSEC2 Link/Speed	Front panel Integrated RJ45 LED (Left)	Off Amber Green	No link 10/100BASE-T operation 1000BASE-T operation
GENET2 ACT	TSEC2 Activity	Front panel Integrated RJ45 LED	Off Blinking Green	No activity Activity proportional to bandwidth utilization

3.3.2 Onboard LEDs

The onboard LEDs are listed below. The LEDs are located on the rear side of the board just opposite of the battery location. To view the board, see Figure 3-1 on page 41.

Figure 3-5 Onboard LEDs

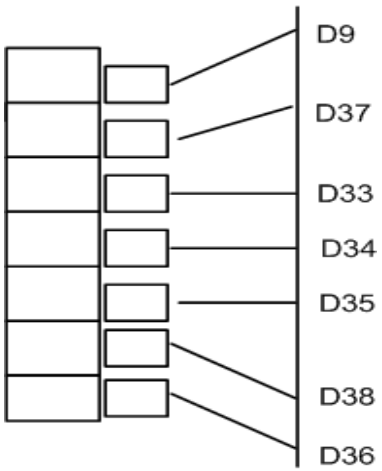


Table 3-2 Onboard LEDs Status

Label	Function	Color	Description
D9	Power Fail	Red	This indicator is illuminated when one or more of the on-board voltage rails fails.
D33	User Defined	Amber	Controlled by the CPLD. Used for boot-up sequence indicator.
D34	User Defined	Amber	Controlled by the CPLD. Used for boot-up sequence indicator.
D35	User Defined	Amber	Controlled by the CPLD. Used for boot-up sequence indicator.
D36	Early Power Fail	Amber	This indicator is lit when the early 3.3V power supply fails.
D37	User Defined	Amber	Controlled by the CPLD
D38	User Defined	Amber	Controlled by the CPLD

3.4 Connectors

This section describes the pin assignments and signals for the connectors on the MVME2502.

3.4.1 Front Panel Connectors

The following connectors are found on the outside of the MVME2502. These connectors are divided between the front panel connectors and the backplane connectors. The front panel connectors include the J1 and J5 connectors. The backplane connectors include the P1 and P2 connectors.

3.4.1.1 RJ45 with Integrated Magnetics (J1)

The MVME2502 uses an X2 RJ45.

Table 3-3 Front Panel Tri-Speed Ethernet Connector (J1)

Pin Name	Signal Description
1A	GND
2A	NC
3A	Port A TRD3 -
4A	Port A TRD3 +
5A	Port A TRD2 -
6A	Port A TRD2 +
7A	Port A TRD1 -
8A	Port A TRD1 +
9A	Port A TRD0 -
10A	Port A TRD0 +
D1A	Port A Green LED1 Anode/ Yellow LED1 Cathode
D2A	Port A Yellow LED1 Anode/ Green LED1 Cathode
D3A	Port A Green LED2 Anode/ Yellow LED2 Cathode
D4A	Port A Yellow LED2 Anode/ Green LED2 Cathode
1B	GND

Table 3-3 Front Panel Tri-Speed Ethernet Connector (J1) (continued)

Pin Name	Signal Description
2B	NC
3B	Port B TRD3 -
4B	Port B TRD3 +
5B	Port B TRD2 -
6B	Port B TRD2 +
7B	Port B TRD1 -
8B	Port B TRD1 +
9B	Port B TRD0 -
10B	Port B TRD0 +
D1B	Port B Green LED1Anode/ Yellow LED1 Cathode
D2B	Port B Yellow LED1 Anode/ Green LED1 Cathode
D3B	Port B Green LED2Anode/ Yellow LED2 Cathode
D4B	Port B Yellow LED2 Anode/ Green LED2 Cathode

3.4.1.2 Front Panel Serial Port (J4)

There is one front access asynchronous serial port interface labeled COMM1 that is routed to the micro mini DB-9 front panel connector. A male-to-male micro-mini DB9 adapter cable is available under Artesyn Embedded Technologiespart number SERIAL-MINI-D (30-W2400E01A). The pin assignments for these connectors are as follows:

Table 3-4 Front Panel Serial Port (J4)

Pin	Signal Description
1	NC
2	RX
3	TX
4	NC
5	GND
6	NC

Table 3-4 Front Panel Serial Port (J4)

Pin	Signal Description
7	RTS
8	CTS
9	NC

3.4.1.3 USB Connector (J5)

The MVME2502 uses upright USB receptacle mounted in the front panel.

Table 3-5 USB Connector (J5)

Pin Name	Signal Description
1	+5 V
2	Data -
3	Data +
4	GND
MTG	Mounting Ground
MTG	Mounting Ground
MTG	Mounting Ground
MTG	Mounting Ground

3.4.1.4 VMEBus P1 Connector

The VME P1 connector is a 160-pin DIN. The P1 connector provides power and VME signals for 24-bit address and 16-bit data. The pin assignments for the P1 connector is as follows:

Table 3-6 VMEbus P1 Connector

Pin	Row A	Row B	Row C	Row D	Row Z
1	DATA 0	BBSY	DATA 8	+5V	NC
2	DATA 1	BCLR	DATA 9	GND	GND
3	DATA 2	ACFAIL	DATA 10	NC	NC

Table 3-6 VMEbus P1 Connector (continued)

Pin	Row A	Row B	Row C	Row D	Row Z
4	DATA 3	BGIN0	DATA 11	NC	GND
5	DATA 4	BGOUT0	DATA 12	NC	NC
6	DATA 5	BGIN1	DATA 13	NC	GND
7	DATA 6	BGOUT1	DATA 14	NC	NC
8	DATA 7	BGIN2	DATA 15	NC	GND
9	GND	BGOUT2	GND	GAP	NC
10	SYSCLK	BGIN3	SYSFAIL	GA0	GND
11	GND	BGOUT3	BERR	GA1	NC
12	DS1	BR0	SYSRESET	+3.3V (not used)	GND
13	DS0	BR1	LWORD	GA2	NC
14	WRITE	BR2	AM 5	+3.3V (not used)	GND
15	GND	BR3	ADD 23	GA3	NC
16	DTACK	AM 0	ADD 24	+3.3V (not used)	GND
17	GND	AM 1	ADD 25	GA4	NC
18	AS	AM 2	ADD 26	+3.3V (not used)	GND
19	GND	AM 3	ADD 27	NC	NC
20	IACK	GND	ADD 28	+3.3V (not used)	GND
21	IACKIN	NC	ADD 29	NC	NC
22	IACKOUT	NC	ADD 30	+3.3V (not used)	GND
23	AM 4	GND	ADD 31	NC	NC
24	ADD 7	IRQ7	ADD 32	+3.3V (not used)	GND
25	ADD 6	IRQ6	ADD 33	NC	NC
26	ADD 5	IRQ5	ADD 34	+3.3V (not used)	GND
27	ADD 4	**IRQ4**	ADD 35	NC	NC
28	ADD 3	IRQ3	ADD 36	+3.3V (not used)	GND
29	ADD 2	IRQ2	ADD 37	NC	NC
30	ADD 1	IRQ1	ADD 38	+3.3V (not used)	GND

Table 3-6 VMEbus P1 Connector (continued)

Pin	Row A	Row B	Row C	Row D	Row Z
31	-12V	NC	+12V	+12V	NC
32	+5V	+5V	+5V	+5V	GND

3.4.1.5 VMEBus P2 Connector

The VME P2 connector is a 160-pin DIN. Row B of the P2 connector provides power to the MVME2502 and to the upper eight VMEbus address lines and additional 16 VMEbus data lines. The Z, A, C, and D pin assignments for the P2 connector are the same for both the MVME2502 and MVME7216E/ MVME721E, and are as follows:

Table 3-7 VMEbus P2 Connector

Pin	Row A	Row B	Row C	Row D	Row Z
1	PMC IO 2	+5V	PMC IO 1	GE3_0 +	Serial 1 RX
2	PMC IO 4	GND	PMC IO 3	GE3_0 -	GND
3	PMC IO 6	RETRY	PMC IO 5	GND	Serial 1 TX
4	PMC IO 8	ADDRESS 24	PMC IO 7	GE3_1 +	GND
5	PMC IO 10	ADDRESS 25	PMC IO 9	GE3_1 -	Serial 1 CTS
6	PMC IO 12	ADDRESS 26	PMC IO 11	GND	GND
7	PMC IO 14	ADDRESS 27	PMC IO 13	GE3_2 +	Serial 1 RTS
8	PMC IO 16	ADDRESS 28	PMC IO 15	GE3_2 -	GND
9	PMC IO 18	ADDRESS 29	PMC IO 17	GND	Serial 2 RX
10	PMC IO 20	ADDRESS 30	PMC IO 19	GE3_3 +	GND
11	PMC IO 22	ADDRESS 31	PMC IO 21	GE3_3 -	Serial 2 TX
12	PMC IO 24	GND	PMC IO 23	GND	GND
13	PMC IO 26	+5V	PMC IO 25	I2C DATA	Serial 2 CTS
14	PMC IO 28	DATA 16	PMC IO 27	I2C CLK	GND
15	PMC IO 30	DATA 17	PMC IO 29	GE3_LINK_ LED	Serial 2 RTS
16	PMC IO 32	DATA 18	PMC IO 31	GE3_ACT_LED	GND
17	PMC IO 34	DATA 19	PMC IO 33	GE4_LINK_LED	Serial 3 RX

Table 3-7 VMEbus P2 Connector (continued)

Pin	Row A	Row B	Row C	Row D	Row Z
18	PMC IO 36	DATA 20	PMC IO 35	GE4_A_LED	GND
19	PMC IO 38	DATA 21	PMC IO 37	GND	Serial 3 TX
20	PMC IO 40	DATA 22	PMC IO 39	GE4_3 -	GND
21	PMC IO 42	DATA 23	PMC IO 41	GE4_3 +	Serial 3 CTS
22	PMC IO 44	GND	PMC IO 43	GND	GND
23	PMC IO 46	DATA 24	PMC IO 45	GE4_2 -	Serial 3 RTS
24	PMC IO 48	DATA 25	PMC IO 47	GE4_2+	GND
25	PMC IO 50	DATA 26	PMC IO 49	GND	Serial 4 RX
26	PMC IO 52	DATA 27	PMC IO 51	GE4_1 -	GND
27	PMC IO 54	DATA 28	PMC IO 53	GE4_1 +	Serial 4 TX
28	PMC IO 56	DATA 29	PMC IO 55	GND	GND
29	PMC IO 58	DATA 30	PMC IO 57	GE4_0 -	Serial 4 CTS
30	PMC IO 60	DATA 31	PMC IO 59	GE4_0 +	GND
31	PMC IO 62	GND	PMC IO 61	GND	Serial 4 RTS
32	PMC IO 64	+5V	PMC IO 63	+5V	GND

3.4.2 Onboard Connectors

3.4.2.1 SATA Connector (J3)

The onboard customized SATA connector is compatible with SATA kit, namely VME-64GBSSDKIT and IVME7210-MNTKIT.

Table 3-8 Custom SATA Connector (J3)

Pin	Signal Description	Pin	Signal Description
1	GND	21	GND
2	GND	22	SATA POWER ENABLE
3	NC	23	NC

Table 3-8 Custom SATA Connector (J3) (continued)

Pin	Signal Description	Pin	Signal Description
4	SATA TX +	24	SATA DETECT
5	NC	25	NC
6	SATA TX -	26	GND
7	GND	27	NC
8	GND	28	GND
9	GND	29	GND
10	GND	30	GND
11	NC	31	+3.3V
12	SATA RX -	32	+5V
13	NC	33	+3.3V
14	SATA RX +	34	+5V
15	GND	35	+3.3V
16	GND	36	+5V
17	NC	37	+3.3V
18	GND	38	+5V
19	NC	39	+3.3V
20	GND	40	+5V

3.4.2.2 PMC Connectors

The MVME2502 supports twoPMC sites. It utilizes J14 to support PMC I/O that goes to the RTM PMC. The tables below show the pin out detail of J11/J111, J12/J222, J13/J333 and J14. See Figure 3-1 for the location of the PMC connectors.

Table 3-9 PMC J11/J111 Connector

Pin	Signal Description	Pin	Signal Description
1	JTAG TCK	33	FRAME
2	-12V	34	GND

Table 3-9 PMC J11/J111 Connector (continued)

Pin	Signal Description	Pin	Signal Description
3	GND	35	GND
4	INT A	36	IRDY
5	INT B	37	DEVSEL
6	INT C	38	+5V
7	PRESENT SIGNAL	39	PCIXCAP
8	+5V	40	LOCK
9	INT D	41	NC
10	NC	42	NC
11	GND	43	PAR
12	NC	44	GND
13	PCI CLK	45	+3.3V
14	GND	46	AD 15
15	GND	47	AD 12
16	GNT A	48	AD 11
17	REQ A	49	AD 9
18	+5V	50	+5V
19	+3.3V	51	GND
20	AD 31	52	CBE0
21	AD 28	53	AD 6
22	AD 27	54	AD 5
23	AD 25	55	AD 4
24	GND	56	GND
25	GND	57	+3.3V
26	CBE3	58	AD 3
27	AD 22	59	AD 2
28	AD 21	60	AD 1
29	AD 19	61	AD 0

Table 3-9 PMC J11/J111 Connector (continued)

Pin	Signal Description	Pin	Signal Description
30	+5V	62	+5V
31	+3.3V	63	GND
32	AD 17	64	REQ64

Table 3-10 PMC J12/J222 Connector

Pin	Signal Description	Pin	Signal Description
1	+12V	33	GND
2	JTAG TRST	34	IDSELB
3	JTAG TMS	35	TRDY
4	JTAG TDO	36	+3.3V
5	JTAG TDI	37	GND
6	GND	38	STOP
7	GND	39	PERR
8	NC	40	GND
9	NC	41	+3.3V
10	NC	42	SERR
11	BUSMODE2 (Pulled UP)	43	CBE1
12	+3.3V	44	GND
13	PCI RESET	45	AD 14
14	BUSMODE3 (PULLED DWN)	46	AD 13
15	+3.3V	47	M66EN
16	BUSMODE4 (PULLED DWN)	48	AD 10
17	NC	49	AD 8
18	GND	50	+3.3V
19	AD 30	51	AD 7
20	AD 29	52	REQB
21	GND	53	+3.3V

Table 3-10 PMC J12/J222 Connector (continued)

Pin	Signal Description	Pin	Signal Description
22	AD 26	54	GNTB
23	AD 24	55	NC
24	+3.3V	56	GND
25	IDSEL	57	NC
26	AD 23	58	EREADY
27	+3.3V	59	GND
28	AD 28	60	RSTOUT
29	AD 18	61	ACK64
30	GND	62	+3.3V
31	AD 16	63	GND
32	CBE2	64	NC

Table 3-11 PMC J13/J333 Connector

Pin	Signal Description	Pin	Signal Description
1	NC	33	GND
2	GND	34	AD48
3	GND	35	AD 47
4	CBE7	36	AD 52
5	CBE6	37	AD 45
6	CBE5	38	GND
7	CBE4	39	+3.3V
8	GND	40	AD 40
9	+3.3V	41	AD 43
10	PAR64	42	AD 42
11	+3.3V	43	AD 41
12	AD 62	44	GND
13	AD 61	45	GND

Table 3-11 PMC J13/J333 Connector (continued)

Pin	Signal Description	Pin	Signal Description
14	GND	46	AD 40
15	GND	47	AD 39
16	AD 60	48	AD 38
17	AD 59	49	AD 37
18	AD 58	50	GND
19	AD 57	51	GND
20	GND	52	AD 36
21	+3.3V	53	AD 35
22	AD 56	54	AD 34
23	AD 55	55	AD 33
24	AD 54	56	GND
25	AD 53	57	+3.3V
26	GND	58	AD 32
27	GND	59	NC
28	GND	60	NC
29	AD 51	61	NC
30	AD 50	62	GND
31	AD 49	63	GND
32	GND	64	NC

Table 3-12 PMC J14 Connector

Pin	Signal Description	Pin	Signal Description
1	PMC IO 1	33	PMC IO 33
2	PMC IO 2	34	PMC IO 34
3	PMC IO 3	35	PMC IO 35
4	PMC IO 4	36	PMC IO 36
5	PMC IO 5	37	PMC IO 37

Table 3-12 PMC J14 Connector (continued)

Pin	Signal Description	Pin	Signal Description
6	PMC IO 6	38	PMC IO 38
7	PMC IO 7	39	PMC IO 39
8	PMC IO 8	40	PMC IO 40
9	PMC IO 9	41	PMC IO 41
10	PMC IO 10	42	PMC IO 42
11	PMC IO 11	43	PMC IO 43
12	PMC IO 12	44	PMC IO 44
13	PMC IO 13	45	PMC IO 45
14	PMC IO 14	46	PMC IO 46
15	PMC IO 15	47	PMC IO 47
16	PMC IO 16	48	PMC IO 48
17	PMC IO 17	49	PMC IO 49
18	PMC IO 18	50	PMC IO 50
19	PMC IO 19	51	PMC IO 51
20	PMC IO 20	52	PMC IO 52
21	PMC IO 21	53	PMC IO 53
22	PMC IO 22	54	PMC IO 54
23	PMC IO 23	55	PMC IO 55
24	PMC IO 24	56	PMC IO 56
25	PMC IO 25	57	PMC IO 57
26	PMC IO 26	58	PMC IO 58
27	PMC IO 27	59	PMC IO 59
28	PMC IO 28	60	PMC IO 60
29	PMC IO 29	61	PMC IO 61
30	PMC IO 30	62	PMC IO 62
31	PMC IO 31	63	PMC IO 63
32	PMC IO 32	64	PMC IO 64

3.4.2.3 JTAG Connector (P6)

The JTAG Connector can be used in conjunction with the JTAG board and ASSET hardware.

Table 3-13 JTAG Connector (P6)

Pin	Signal Description	Pin	Signal Description
1	NC	2	+3.3V FROM +5V
3	SPI HOLD 0	4	SPI CS 0
5	SPI CLK	6	SPI CS 1
7	SPI HOLD 1	8	SPI MOSI
9	SPI MISO	10	GND
11	SPI VCC	12	SCAN 1 TCK
13	SCAN 1 TDI	14	GND
15	SCAN 1 TRST	16	SCAN 1 TDO
17	SCAN 1 TMS	18	+3.3V
19	GPO0	20	NC
21	NC	22	SCAN 2 TMS
23	NC	24	SCAN 2 TDO
25	SCAN 2 TCK	26	+3.3V FROM +5V
27	GND	28	SCAN 2 TDI
29	NC	30	NC
31	SCAN 3 TMS	32	SCAN 3 TCK1
33	SCAN 3 TDO	34	SCAN 3 TCK 2
35	+2.5V	36	SCAN 3 TCK 3
37	SCAN 3 TDI	38	GND
39	SCAN 3 TRST	40	SCAN 3 TCK3
41	SCAN 4 TCK 1	42	SCAN 4 TMS
43	GND	44	SCAN 4 TDO
45	SCAN 4 TCK 2	46	+3.3V
47	GND	48	SCAN 4 TDI

Table 3-13 JTAG Connector (P6) (continued)

Pin	Signal Description	Pin	Signal Description
49	SCAN 4 TCK 3	50	SCAN 4 TRST
51	SCAN 5 TMS	52	SCAN 5
53	SCAN 5 TDO	54	GND
55	+3.3V	56	SCAN5 TCK2
57	SCAN 5 TDI	58	GND
59	SCAN 5 TRST	60	NC

3.4.2.4 COP Connector (P6)

The COP header is used for the CPU debug. The pin assignment is dictated by Freescale and is compatible with the processor's debugging tool.

Table 3-14 COP Header (P10)

Pin	Signal Description
1	JTAG TDI
2	COP QACK
3	JTAG TDO
4	COP TRST
5	COP RUNSTOP (Pulled UP)
6	COP VDD SENSE
7	JTAG TCK
8	COP CHECK STOP IN
9	JTAG TMS
10	NC
11	P2020 SW RESET
12	COP PRESENT
13	COP HARD RESET
14	KEYING

Table 3-14 COP Header (P10)

Pin	Signal Description
15	COP CHECK STOP OUT
16	GND

3.4.2.5 XMC Connector (XJ1)

The MVME2502 supports two XMC sites. The board only support J15 for XMC site 1 and J25 for XMC site 2.

Table 3-15 XMC Connector (XJ1) Pin out

Pin	Row A	Row B	Row C	Row D	Row E	Row F
1	RX0 +	RX0 -	+3.3V	NC	NC	+3.3V
2	GND	GND	JTAG TRST	GND	GND	HRESET
3	NC	NC	+3.3V	NC	NC	+3.3V
4	GND	GND	JTAG TCK	GND	GND	MRSTO (PULLED UP)
5	NC	NC	+3.3V	NC	NC	+3.3V
6	GND	GND	JTAG TMS	GND	GND	+12V
7	NC	NC	+3.3V	NC	NC	+3.3V
8	GND	GND	JTAG TMS	GND	GND	-12V
9	NC	NC	NC	NC	NC	+3.3V
10	GND	GND	JTAG TDO	GND	GND	GA 0
11	TX0	TX0 -	BIST (PULLED UP)	NC	NC	+3.3V
12	GND	GND	GA 1	GND	GND	PRESENT
13	NC	NC	NC	NC	NC	+3.3V
14	GND	GND	GA 2	GND	GND	I2C DATA
15	NC	NC	NC	NC	NC	+3.3V
16	GND	GND	MVMRO (PULLED DOWN)	GND	GND	I2C CLOCK

Table 3-15 XMC Connector (XJ1) Pin out (continued)

Pin	Row A	Row B	Row C	Row D	Row E	Row F
17	NC	NC	NC	NC	NC	NC
18	GND	GND	NC	GND	GND	NC
19	CLK +	CLK -	NC	ROOT 0 (PULLED UP)	ROOT0 (PULLED UP)	NC

3.4.2.6 XMC Connector (XJ2)

Table 3-16 XMC Connector (XJ2) Pin out

Pin	Row A	Row B	Row C	Row D	Row E	Row F
1	RX0 +	RX0 -	+3.3V	RX1+	RX1-	+3.3V
2	GND	GND	JTAG TRST	GND	GND	HRESET
3	NC	NC	+3.3V	NC	NC	+3.3V
4	GND	GND	JTAG TCK	GND	GND	MRSTO (PULLED UP)
5	NC	NC	+3.3V	NC	NC	+3.3V
6	GND	GND	JTAG TMS	GND	GND	+12V
7	NC	NC	+3.3V	NC	NC	+3.3V
8	GND	GND	JTAG TMS	GND	GND	-12V
9	NC	NC	NC	NC	NC	+3.3V
10	GND	GND	JTAG TDO	GND	GND	GA 0
11	TX0	TX0 -	BIST (PULLED UP)	TX1+	TX1-	+3.3V
12	GND	GND	GA 1	GND	GND	PRESENT
13	NC	NC	NC	NC	NC	+3.3V
14	GND	GND	GA 2	GND	GND	I2C DATA
15	NC	NC	NC	NC	NC	+3.3V

Table 3-16 XMC Connector (XJ2) Pin out (continued)

Pin	Row A	Row B	Row C	Row D	Row E	Row F
16	GND	GND	MVMRO (PULLED DOWN)	GND	GND	I2C CLOCK
17	NC	NC	NC	NC	NC	NC
18	GND	GND	NC	GND	GND	NC
19	CLK +	CLK -	NC	NC	ROOT0 (PULLED UP)	NC

3.4.2.7 Miscellaneous P2020 Debug Connectors

Table 3-17 P2020 Debug Header

Pin	Signal Description
1	MSRCDI0
2	GND
3	MSRCDI1
4	MDVAL
5	MSRCDI2
6	TRIG_OUT
7	MSRCDI3
8	TRIG_IN
9	MSRCID4
10	GND

3.5 Switches

These switches control the configuration of the MVME2502.

NOTICE

Board Malfunction

- Switches marked as “reserved” might carry production-related functions and can cause the board to malfunction if their settings are changed.
- Do not change settings of switches marked as “reserved”. The setting of switches which are not marked as “reserved” has to be checked and changed before board installation.

3.5.1 Geographical Address Switch (S1)

The Tsi148 VMEbus Status Register provides the VMEbus geographical address of the MVM2502. The switch reflects the inverted states of the geographical address signals. Applications not using the five row backplane can use the geographical address switch to assign a geographical address based on the following diagram.

Note that this switch is wired in parallel with the geographical address pins on the five row connector. These switches must be in the "OFF" position when installed in a five row chassis in order to get the correct address from the P1 connector. This switch also includes the SCON control switches.

Figure 3-6 Geographical Address Switch

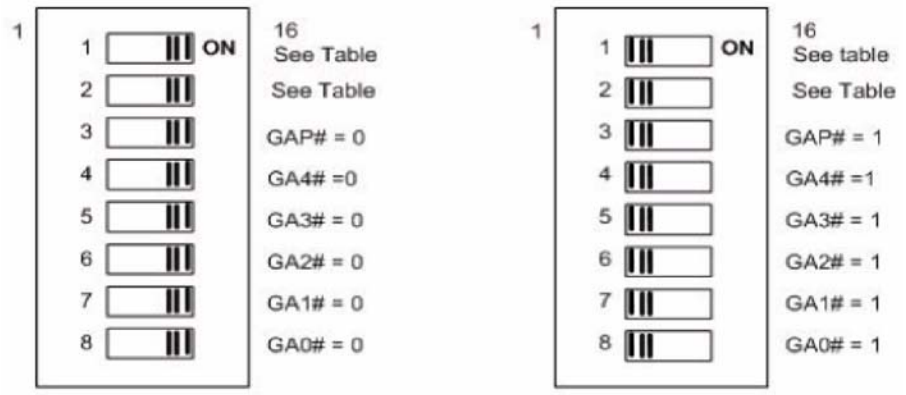


Table 3-18 Geographical Address Switch

Position	Function	Default
S1-1	VME SCON Auto[1]	Auto-SCON
S1-2	VME SCON SEL[2]	Non-SCON
S1-3	GAP	1
S1-4	GA4	1
S1-5	GA3	1
S1-6	GA2	1
S1-7	GA1	1
S1-8	GA0	1

1. The VME SCON MAN switch is "OFF" to select Auto-SCON mode. The switch is "ON" to select manual SCON mode which works in conjunction with the VME SCON SEL switch.

2. The VME SCON SEL switch is OFF to select non-SCON mode. The switch is ON to select always SCON mode. This switch is only effective when the VME SCON MAN switch is "ON".

3.5.2 SMT Configuration Switch (S2)

This eight position SMT configuration switch controls the flash bank user defined switch, selects the flash boot image, and controls the safe start ENV settings. The default setting on all switch positions is "OFF" and is indicated by brackets in Table 3-19.

Figure 3-7 SMT Configuration Switch Position

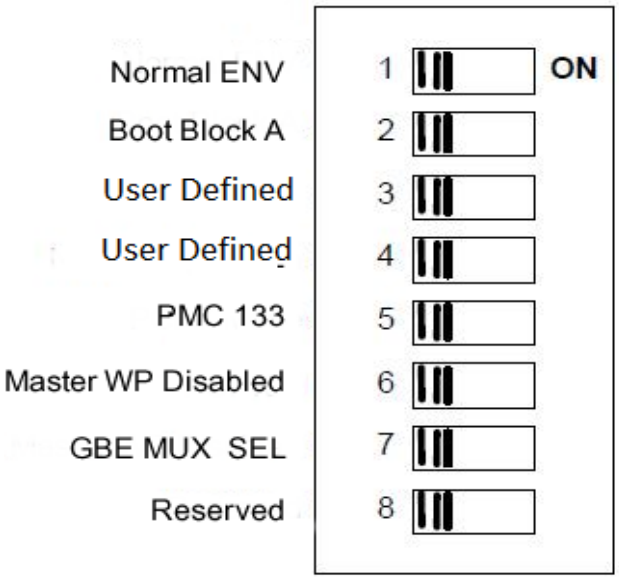


Table 3-19 Geographical Address Switch Settings

SW2	DEFAULT	Signal Name	Description	Notes
1	OFF (Normal Env)	NORMAL_ENV	Safe Start ("ON"= Use normal ENV, "OFF"= Use safe ENV)	
2	OFF (Flash Block A)	BOOT_BLOCK_A	Boot Block B Select	
3	OFF (User defined)	FLASH_WP_N	User defined	
4	OFF (User defined)	PMC_XMC_SEL	User defined	Will select if XMC card or PMC card is used
5	OFF (133 MHz)	PMC_133	PCI frequency selection	

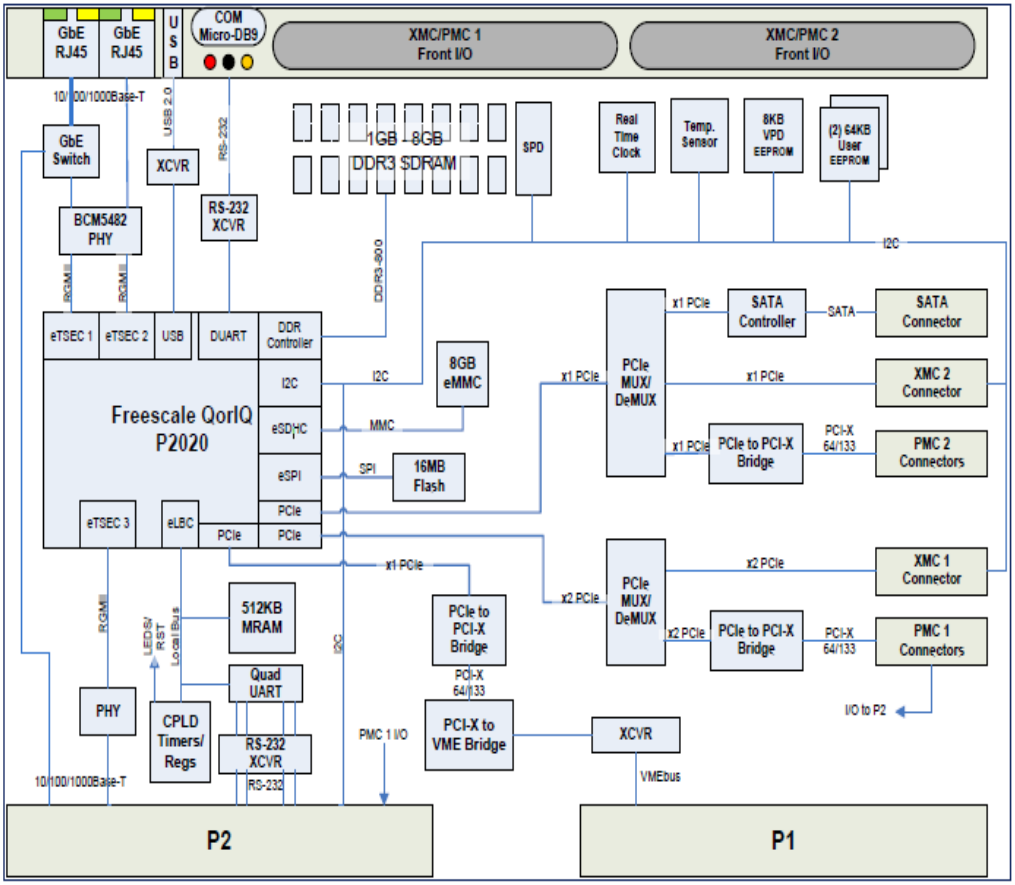
Table 3-19 Geographical Address Switch Settings (continued)

SW2	DEFAULT	Signal Name	Description	Notes
6	OFF (WP Enabled)	MASTER_WP_DISABLED	EEPROM Write-Protect	For I2C write-protect only.
7	OFF (Front)	GBE_MUX_SEL	User Defined switch that will select if the GBE PHY will function on the front panel or on the Back PLANE	
8	OFF (CPU Reset Deasserted)	Reserved		Should be "OFF" for normal operation.

4.1 Block Diagram

The MVME2502 block diagram is illustrated in Figure 4-1. All variants provide front panel access to one serial port via a micro-mini DB-9 connector, two 10/100/1000 Ethernet port (one is configurable to be routed on the front panel or to the rear panel) through a ganged RJ45 connector and one Type A USB Port. It includes Board Fail LED indicator, user-defined LED indicator and a ABORT/RESET switch.

Figure 4-1 Block Diagram



4.2 Chipset

The MVME2502 utilizes the QorIQ P2020 integrated processor. It offers an excellent combination of protocol and interface support including dual high performance CPU cores, a large L2 cache, a DDR2/DDR3 memory controller, three enhanced three-speed Ethernet controllers, two Serial RapidIO interfaces with a messaging unit, a secure digital interface, a USB 2.0 interface and three PCI express controllers.

This section describes the protocol and interfaces provided in the QorIQ P2020 integrated and is utilized by the MVME2502.

4.2.1 e500 Processor Core

The QorIQ integrated processors offer dual high performance e500v2 core (P2020). It operates from 1.0GHz up to 1.2GHz core frequency. The e500 processor core is a low-power implementation of the family of reduced instruction set computing (RISC) embedded processor that implement the Book E definition of the PowerPC architecture. The e500 is a 32-bit implementation of the Book E architecture using the lower words of 64-bit general-purpose registers (GPRs) while E500v2 uses 36 bit physical addressing and some improvement from the previous version.

4.2.2 Integrated Memory Controller

A fully programmable DDR SDRAM controller supports most JEDEC standard DDR2 and DDR3 memories available. A built-in error checking and correction (ECC) ensures very low bit-error rates for reliable high-frequency operation. ECC is implemented on MVME2502.

The memory controller supports the following:

- 16 GB of memory
- Asynchronous clocking from platform clock, with programmable settings that meets all the SDRAM timing parameters.
- Up to four physical banks; each bank can be independently addressed to 64 Mbit to 4 Gbit memory devices (depending on the internal device configuration with x8/x16/x32 data ports).
- Chip set interleaving and partial array self-refresh.
- Data mask signal and read-modify-write for sub-double-word writes when ECC is enabled.

- Double-bit error detection and single-bit error correction ECC, 8-bit check work across 64-bit data.
- Automatic DRAM initialization sequence or software-controlled initialization sequence and automatic DRAM data initialization.
- Write leveling for DDR3 memories and supports up to eight posted refreshes.

4.2.3 PCI Express Interface

The PCI Express interface is compatible with the PCI Express Base Specification Rev. 1.0a. The PCI Express controller connects the internal platform to a 2.5 GHz serial interface. The P2020 has the options for up to three PCIe interfaces with up to x4 link width. The PCIe controller can be configured to operate as either PCIe root complex (RC) or as an endpoint (EP) device.

4.2.4 Local Bus Controller (LBC)

The main component of the enhanced LBC is the memory controller that provides a 16-bit interface to various types of memory devices and peripherals. The memory controller is responsible for controlling eight memory banks shared by the following: a general purpose chip select machine (GPCM); a flash controller machine (FCM) and user programmable machines (UPMs). The MVME2502 supports the GPCM, to interface with the CPLD, MRAM and QUART.

4.2.5 Secure Digital Host Controller (SDHC)

The ENP1 and ENP2 variants of the MVME2502 use a soldered down 8GB eMMC device connected to the SDHC interface of the P2020 Processor. This is the only device available on the SDHC interface.

4.2.6 I^2C Interface

The MVME2502 has two independent I^2C buses on the processor. The MVME2502 use port 2 for the XMC modules and I2C port 1 for all other devices. For more information, see *I2C Devices, on page 86*.

4.2.7 USB Interface

The P2020 implements a USB 2.0 compliant serial interface engine. For more information, see *USB, on page 85*.

4.2.8 DUART

The chipset provides two universal asynchronous receiver/transmitter (UART). Each UART is clocked by the CCB clock and is compatible with PC16522D. As a full-duplex interface, it provides a 16-byte FIFO for both transmitter and receiver mode.

4.2.9 DMA Controller

The DMA controller transfers blocks of data between the various interfaces and functional blocks of P2020 that are independent of the e500 cores. The P2020 DMA controller has three high-speed DMA channels, all of which capable of complex data movement and advanced transaction chaining.

4.2.10 Enhanced Three-Speed Ethernet Controller (eTSEC)

The eTSEC controller of the device interface to10 Mbps, 100 Mbps, and 1 Gbps Ethernet/IEE 802.3 networks, and devices featuring generic 8 to 16-bit FIFO ports. The MVME2502 uses the eTSEC using the RGMII interface.

4.2.11 General Purpose I/O (GPIO)

The P2020 has a total of sixteen I/O ports. Four of these ports are used alternately as external input interrupt. All sixteen ports have open drain capabilities.

The table below details the GPIO usage for the MVME2502:

Table 4-1 P2020 GPIO Functions

GPIO bit	CPU Pin #	Function
15	E24	Not connected
14	F24	Not connected

Table 4-1 P2020 GPIO Functions

GPIO bit	CPU Pin #	Function
13	E23	Connected to pin R7 of the CPLD (unused input)
12	F23	Connected to pin M8 of the CPLD (unused input)
11	D24	Connected to pin M7 of the CPLD (unused input)
10	A25	Not connected
09	A24	Not connected
08	F22	Not connected
07	R25	Not connected
06	R29	Connected to pin T6 of the CPLD (unused input)
05	R24	Connected to pin R6 of the CPLD (unused input)
04	U29	Connected to INTA of the QUART. Programmed as a discrete input or to generate IRQ11. Also connected to pin P16 of the CPLD. (unused input)
03	N24	Connected to pin P15of the CPLD
02	P29	Connected to Pin R16 of the CPLD. Programmed to generate a IRQ09 interrupt to the CPU based on contents of the CPLD GPIO2 interrupt register. For more information see, *PLD GPIO2 Interrupt Register* on page 109.
01	R26	Connected to INTA_N of the DS1337 Real Time Clock (RTC). Programmed as a discrete input or to generate IRQ08
00	R28	Connected to LED_P21[2] of the BCM5482S. Programmed as a discrete input or to generate IRQ07.

4.2.12 Security Engine (SEC) 3.1

The integrated security engine of the P2020 is designed to off-load intensive security functions like key generation and exchange, authentication and bulk encryption from the processor core. It includes eight different execution units where data flows in and out of an EU.

NOTE: The standard versions of the MVME2502 do not use the encryption enabled versions of the P2020 processor.

4.2.13 Common On-Chip Processor (COP)

The COP is the debug interface of the QorIQ P2020 Processor. It allows a remote computer system to access and control the internal operation of the processor. The COP interface connects primarily through the JTAG and has additional status monitoring signals. The COP has additional features like breakpoints, watch points, register and memory examination/modification and other standard debugging features.

4.2.14 P2020 Strapping Pins

The following table lists all the P2020 strapping pins and the default configuration settings for the MVME2502.

Table 4-2 P2020 Strapping Options

Functional Signal Name	Reset Configuration Name	Config Resistor Options	Default Value	Description
LA[29:31]	cfg_sys_pii[0:2]	Yes	000	4:1 ratio CCB clock: SYSCLK =100MHz, CCB=400Mhz
TSEC_1588_CLKOUT TSEC_1588_PULSE_OUT1 TSEC_1588_PULSE_OUT2	cfg_ddr_pii[0:2]	Yes	011	8:1 ratio, DDRCLK=100MHz, DDRPLL (data rate) = 800MHz
LBCTL LALE LGPL2/LOE/LFRE	cfg_core0pii[0:2]	Yes	110 101	ENP1: 3:1 ratio, CCB clock= 400MHz, Core clock=1200MHz
				ENP2: 2.5:1 ratio, CCB clock= 400MHz, Core clock=1000MHz

Table 4-2 P2020 Strapping Options

Functional Signal Name	Reset Configuration Name	Config Resistor Options	Default Value	Description
LWE0_N UART_SOUT1 READY_P1	cfg_core1pii[0:2]	Yes	110	ENP1: 3:1 ratio, CCB clock= 400MHz, Core clock=1200MHz
			101	ENP2: 2.5:1 ratio, CCB clock= 400MHz, Core clock=1000MHz
LA27 LA16	cfg_cup0_boot cfg_cpu1_boot	Yes	10	CPU0 boot without waiting. CPU1 holdoff
LGPL3/LFW PLGPL5	cfg_boot_seq[0:1]	Yes	11	Boot sequencer is disabled. No I2C ROM is accessed (default)
DMA2_DACK0	cfg_mem_debug	Yes	1	DDR SDRAM controller debug info driven to MSRCID/MDVAL (default)
DMA2_DDONE0	cfg_ddr_debug	Yes	1	Debug information is not driven on ECC pins (default)
EC_MDC	cfg_tsec_reduce	Yes	0	eTSEC1 and eTSEC2 Ethernet interfaces operate in RGMII mode
TSEC1_TXD[0,7]	cfg_tsec1_prctcl[0:1]	Yes	10	The eTSEC1 controller operates using the RGMII protocol
TSEC2_TXD[0,7]	cfg_tsec2_prctcl[0:1]	Yes	10	The eTSEC2 controller operates using the RGMII protocol
UART_RTS0,UART_RTS1	cfg_tsec3_prctcl[0:1]	Yes	10	The eTSEC3 controller operates using the RGMII protocol
TSEC1_TXD[3:1] TSEC2_TX_ERR	cfg_io_ports[0:3]	Yes	0010	PCIE1=1x, PCIE2=1x, PCI3=2x
MSRCID0	cfg_elbc_ecc	Yes	0	eLBC ECC checking is disabled
LA28	cfg_sys_speed	Yes	1	SYSCLK is at or above 66MHz (default)
LA23	cfg_plat_speed	Yes	1	Platform clock is at or above 333MHz (default)

Table 4-2 P2020 Strapping Options

Functional Signal Name	Reset Configuration Name	Config Resistor Options	Default Value	Description
LA24	cfg_core0_speed	Yes	1	ENP1: Core0 clock frequency is greater than 1000MHz
			0	ENP2: Core0 clock frequency is less than or equal to 1000MHz
LA25	cfg_core1_speed	Yes	1	ENP1: Core1 clock frequency is greater than 1000MHz
			0	ENP2: Core1 clock frequency is less than or equal to 1000MHz
LA26	cfg_ddr_speed	Yes	1	DDR Controller complex clock frequency (same as DDR rate) is greater than or equal to 500 MHZ (default)
LVDD_VSEL		Yes	1	eTSEC, ethernet management, 1588 interfaces = 2.5V
BVD_VSEL[0:1]		Yes	11	Local bus and GPIO[8:15] interfaces = 3.3V
CVDD_VSEL[0:1]		Yes	00	USB, eSDHC, SPI interface = 3.3V
LA[20:22] UART_SOUT[0] TRIG_OUT MSRCID[1] MSRCID[4] DMA1_DDONE_B[0]	cfg_en_use[0:7]	Yes	11111111	default
TSEC2_TXD1	cfg_dram_type	Yes	1	DDR3 SDRAM selected 1.5V (default)
TSEC2_TXD5	cfg_sdhc_cd_pol_sel	Yes	1	SDHC polarity detect = not inverted
TSEC1_TXD[6:4] TSEC1_TX_ER	cfg_rom_loc[0:3]	Yes	0110	Location of boot ROM = SPI FLASH

Table 4-2 P2020 Strapping Options

Functional Signal Name	Reset Configuration Name	Config Resistor Options	Default Value	Description
For the following options, no strapping options provided. They are only listed for reference.				
LGPL1	cfg_sgmii2	No	1	eTSEC2 interface operates in parallel interface mode (default)
TSEC_1588_ALARM_OUT2	cfg_sgmii3	No	1	eTSEC3 interface operates in parallel interface mode (default)
TSEC_1588_ALARM_OUT1	cfg_srds_refclk	No	1	100MHz SERDES ref clock for PCIE (default)
LWE1/LBS1 LA[18:19]	cfg_host_agt[0:2]	No	111	Processor acts as the host root complex for all PCIE busses(default)
TSEC2_TXD[4:2]	cfg_device_ID[7:5]	No	111	Rapid IO interface not used => default values used
LAD[0:15]	cfg_gpinput[0:15]	No		No default value. Input pins do not have internal pull-up resistors
LGPL0	cfg_rio_sys_size	No	1	Rapid IO interface not used => default values used

4.3 System Memory

The P2020 integrated memory controller supports both DDR2 and DDR3 memory devices. It has one channel and can be configured up to four memory banks with x8, x16 and x32 devices. Selection of 4GB devices allows support of up to 16 GB of memory. ECC is also supported.

The MVME2502 design implements 2 banks of 9x8 devices which includes ECC. The standard configurations populate a single memory bank of 2Gb DDR3-800 for a 2GB capacity. The MVME2502 is designed to accommodate 4Gb DDR3 devices supporting up to 8 Gb total when both memory banks are populated with 4Gb devices.

4.4 Timers

There are various timer functions implemented on the MVME2502 platform:

4.4.1 Real Time Clock

The MVME-2502 implements a Maxim DS1337 RTC to maintain seconds, minutes, hours, day, date, month, year accurately. The INT_A pin of the DS1337 is connected to the CPU GPIO[1] pin to allow the DS1337 to generate interrupts to the CPU. Access to the DS1337 is provided via the I2C port 0 from the CPU and responds to a base I2C address of $D0.

The MVME2502 provides a socketed 48mAh primary battery to power the RTC when the module is out of service.

4.4.2 P2020 Internal Timer

The processor's internal timer is composed of eight global timers divided into two groups of four timers each. Each time has four individual configuration registers and they cannot be cascaded together.

4.4.3 Watchdog Timer

The onboard CPLD provides programmable 16-bit watchdog timers. It has a 1 ms resolution and generates a board reset when the counter expires. Interrupt is generated to the processor when this occurs. Default value is 60 seconds.

4.4.4 CPLD Tick Timer

The MVME2502 supports three independent 32-bit timers that are implemented on the CPLD to provide fully programmable registers for the timers.

4.5 Ethernet Interfaces

The MVME2502 has three eTSEC controllers. Each one supports RGMII, GMII, and SGMII interface to the external PHY. All controllers can only be utilized when using the RGMII interface. Using the GMII allows only up to two usable controllers.

MVME2502 provides two 10/100/1000 Ethernet interfaces on the front panel and another two are routed to the RTM through the backplane connector. Due to controller limitations, one controller is designed to be routed to the front panel or to the RTM. This setting is possible by using a third party gigabit Ethernet LAN switch with a single enable switch such as PERICOM's P13L301D. The routing direction can be configured through the on-board dip switch.

The registers of the PHY can be accessed through the processor's two-wire Ethernet management interface.The front panel RJ45 connector has integrated speed and activity status indicator LEDs. Isolation transformers are provided onboard for each port.

4.6 SPI Bus Interface

The enhanced serial peripheral interface (eSPI) allows the device to exchange data with peripheral devices such as EEPROMs, RTC, Flash and the like. The eSPI is a full-duplex synchronous, character-oriented channel that supports a simple interface such as receive, transmit, clock and chip selects. The eSPI receiver and transmitter each have a FIFO of 32 Bytes.

P2020 supports up to four chip selects and RapidS full clock cycle operation. It can operate both full-duplex and half duplex. It works with a range from 4-bit to 16-bit data characters and is a single-master environment. MVME2502 is configured such that the eSPI can operate up to 200 MHz clock rate and can support booting process.The firmware boot flash resides in the P2020 eSPI bus interface.

4.6.1 SPI Flash Memory

The MVME2502 has two 8 MB onboard serial flash. Both contain the ENV variables and the U-Boot firmware image, which is about 513 KB in size. Both SPI flash contain the same programming for firmware redundancy and crisis recovery. The SPI flash can be programmed through the JTAG interface or through an onboard SPI flash programming header.

For information on U-boot and ENV Variables location see, *Flash Memory Map*, Table 5-2 on page 96.

4.6.2 SPI Flash Programming

The MVME2502 has three headers: a 10-pin header for SPI Flash programming, an 80-pin header for the JTAG connectivity and a 20-pin JTAG header for ASSET hardware connectivity. The following options are used to program the onboard flash:

- Using onboard SPI header - The MVME2502 uses the 10-pin header with a Dual SPI Flash in-circuit programming configuration. The pin connection is compatible with DediProg SPI Universal Pin Header.
- Using 60-pin external JTAG header - An external JTAG board with a JTAG multiplexer is compatible with the MVME2502 and can be attached using an external cable. It can be used to update the boot loader in the field. Using this method, programming can be done through the JTAG interface or by using the dedicated SPI Flash programming header on the JTAG board.
- Factory Pre-Programming - Programming the SPI Flash usually takes a while. Ideally, the SPI Flash should be pre-programmed in the factory before shipment.
- ICT Programming - This programming is done on exposed test points using a bed of nails tester.

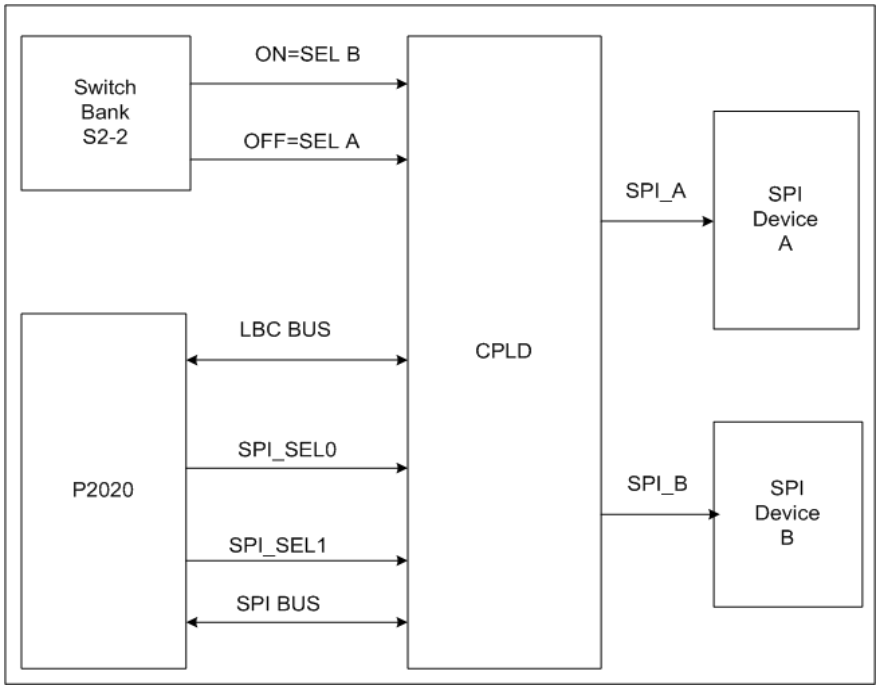
The board power should be switched on before programming. The switch S2-8 should also be powered on to successfully detect the SPI Flash chip.

4.6.3 Firmware Redundancy

The MVME2502 uses two physically separate boot devices to provide boot firmware redundancy. Although the P2020 provides four SPI Bus chip-selects, the P2020 is only capable of booting from the SPI Device controlled by Chip Select 0. External SPI multiplexing logic is implemented on the MVME2502 to accommodate this chipset limitation.

The MVME2502 CPLD controls the chip select to SPI devices A and B. The CPLD chip select control is based on the Switch Bank (S2-2).

Figure 4-2 SPI Device Multiplexing Logic



At power-up, the selection of the SPI boot device is strictly based upon the Switch Bank (S2-2) setting. Depending on the S2-2 setting, SPI_SEL0 is routed to one of two SPI devices. The selected SPI device must contain a boot image. Once the boot image is copied into memory and executed, the CPLD will wait and once the P2020 will write on one bit of the CPLD watchdog register, the CPLD will then pass through the SPI chip select from the P2020 to SPI device chip selects. The software can now perform read/write processes on any SPI device, including copying from one SPI device to another.

With this flexible approach to firmware redundancy, one should always be able to recover from a corrupt active firmware image, as long as a healthy firmware image is maintained in single bootable SPI Device.

The MVME2502 supports automatic switch over. If booting one device is not successful, the watchdog will trigger the board reset and it will automatically boot on the other device.

4.6.4 Crisis Recovery

The MVME2502 provides an independent boot firmware recovery mechanism for the operating system. The firmware recovery can be performed without leaving the firmware environment.

During crisis recovery, the healthy boot image contained in SPI Device B is copied to SPI Device A, replacing the corrupt boot image contained in SPI Device A.

Crisis recovery is performed as follows:

1. Power off the board.
2. Set Switch S2-2 to "ON" to point to SPI Device B (crisis image).
3. Power on the board.
4. Press "h" on the keyboard to go to the U-Boot prompt.
5. Type "moninit fru" to copy the crisis image to SPI Device A.
6. Once the U-Boot prompt is visible, power off the board.
7. Set the S2-3 back to "OFF" to point to the SPI Device A.
8. Power on the board to boot from the newly recovered image on the SPI Device A.

The board will automatically switch over if one of the devices is corrupted.

4.7 Front UART Control

The MVME2502 utilizes one of the two UART functions provided in the male micro-mini DB-9 front panel. A male-to-male micro-mini DB-9 to DB9 adapter cable is available under Artesyn Embedded Technologies Part Number SERIAL-MINI-D (30-W2400E01A) and is approximately 12 inches in length.

Only 115200 bps and 9600 bps are supported. The default baud rate on the front panel serial is 9600 kbps.

4.8 Rear UART Control

The MVME2502 utilizes the Exar ST16C554 quad UART (QUART) to provide four asynchronous serial interface' to the RTM. These devices feature 16 bytes of transmit and receive first-in first-out (FIFO) with selectable receive FIFO trigger levels and data rates of up to 1.5 Mbps. Each UART has a set of registers that provide the user with operating status and control. The QUART are 8-bit devices connected to the processor through the local bus controller using LBC chipset CS1, CS2, CS3 and CS4.

These four serial interfaces are routed to P2 I/O for RTM accessibility. There are a total of five serial ports available on the MVME2502.

4.9 PMC/XMC Sites

The MVME2502 hosts two PMC/XMC sites and accepts either a PMC or an XMC add-on card. Only an XMC or a PMC may be populated at any given time as both occupy the same physical space on the PCB. Combination PMC/XM cards are not supported by the MVME2502. The site provides a rear PMC I/O.

The PMC sites are fully compliant with the following:

1. VITA 39 –PCI-X for PMC.
2. VITA 35-2000 for PMC P4 to VME P2 Connection.
3. PCI Rev 2.2 for PCI Local Bus Specification.
4. PCI-X PT 2.0 for PCI-X Protocol Addendum to the PCI Local Bus Specs.
5. IEEE Standard P1386-2001 for Standard for Common Mezzanine Card Family.
6. IEEE Standard P1386.1-2001 for Standard Physical and Environmental Layer for PCI Mezzanine Card.
7. VITA 42 for XMC.
8. VITA 42.3 , PCIe for XMC.

PMC/XMC sites are keyed for 3.3V PMC signaling. PMC and XMC add-on cards must have a hole in the 3.3 V PMC keying position in order to be populated on the MVME2502. The XMC specification accommodates this since it is expected that carrier cards will host both XMC and PMC capable add-on cards.

The MVME2502 have a keying pin at the 3.3V location at each PMC site. The MVME2502 boards are not 5 volt PMC IO compatible. The MVME2502 also has a 5 volt keying pin location at each PMC site. At PMC site 2, the 5 volt keying pin hole is used to mount the SATA adapter card. Warning label covers 5 volt keying pin at PMC site 1 and also at PMC site 2. If 5 volt PMC or XMC devices are operated on MVME2502 it may cause damage to the board.

The MVME2502 utilizes the P2020 x2 link PCI Express interface for PMC/XMC1 and x1 link PCI Express interface for PMC/XMC2. It is designed such that same PCI Express interface is used for either PMC or XMC. It is made possible by using PCIe Mux/DeMux chip. The CPLD via on-board switch controls the enable pin.

The CPLD controls the PCIe Mux/DeMux at both sites. The CPLD detects the presence signal provided by the XMC or PMC board and it will be used to configure the routing of PCIe Mux/DeMux correspondingly.

4.9.1 PMC Add-on Card

The MVME2502 PMC interface utilizes IDT's TSI384 as the PCIe/PCI-X bridge. It can support up to 8.5 Gbps (64 bits x 133 Mhz). The onboard switch S2-5 configures the TSI384 to run on either 100 Mhz or 133 Mhz, with 133 Mhz as default.

The MVME2502 supports multi-function PMCs and processor PMCs (PrPMCs). The PMC site has two IDSELs, two REQ/GNT pairs, and EREADY to support PrPMC as defined by VITA39.

4.9.2 XMC Add-on Card

The x2 links the PCI-E Gen 1 and is directly routed to the P15 XM connector through Pericom MUX Switch. The onboard switch S2-4 should be set to "ON".

XMC add-on cards are required to operate at +5V or +12V (from carrier to XMC). The MVME2502 provides +5V to the XMC VPWR (Variable Power) pins. The MVME2502 does not provide +12V to the XMC VPWR pins. Voltage tolerances for VPWR and all carrier supplied voltage (+3.3 V, +12 V, -12 V) are defined by the base XMC standard.

4.10 SATA Interface

The MVME2502 supports an optional 2.5" SATA HDD. The connector interface is compatible with the SATAMNKIT, which contains the following: one SSD/HDD, one SATA board, screws and a mounting guide. The SATA connector can support a horizontal mounted SSD/HDD.

The MVME2502 uses Marvell's 88SE9125 SATA controller and supports up to 1.5 Gbps, 3.0 Gbps, or 6.0 Gbps (SATA Gen 1). For status indicators, it has an onboard green LED, D12 and D13 for SATA link and SATA activity status respectively.

4.11 VME Support

The MVME2502 can operate in either System Controller (SCON) mode or non-SCON mode, as determined by the switch setting of S1-1 and S1-2.

The P2020 x1 link is used for the VME backplane connectivity through the Tsi384 (PCI-E/PCI-X) and Tsi148 (PCI-X/VMEBus) bridges.

See *VMEBus P1 Connector, on page 49* and *VMEBus P2 Connector, on page 51* for more information.

4.11.1 Tsi148 VME Controller

The VMEbus interface for the MVME2502 is provided by the Tsi148 VMEbus controller. The Tsi148 provides the required VME, VME extensions, and 2eSST functions. TI SN74VMEH22501transceivers are used to buffer the VME signals between the Tsi148 and the VME backplane. Refer to the Tsi148 user's manual for additional details and/or programming information.

4.12 USB

The MVME2502 processor implements a dual-role (DR) USB 2.0 compliant serial interface engine. DC power to the front panel USB port is supplied using a USB power switch which provides soft-start, current limiting, over current detection, and power enable for port 1.

4.13 I²C Devices

The MVME2502 utilizes two I2C ports provided by the board's processor. The I²C bus is a two-wire, serial data (SDA) and serial clock (SCL), synchronous, multi-master bi-directional serial bus that allows data exchange between this device and other devices such as VPD, SPD, EEPROM, RTC, temperature sensor, RTM, XMC and IDT clocking.

The user can configure the RTM I2C adders and should be aware to avoid address duplication. For more information on I2C bus device addressing, see *I2C Bus Device Addressing* on page 134.

Following are the I2C bus addresses:

Table 4-3 P2020 I2C Port1 Devices

Ref Designator	I2C Device	I2C 8-bit Base Address	Device Type
U39	Temperature Sensor	$98	ADT 7461 Temperature Sensor
U37	SPD	$A0	AT24C02 (256x8)
U40	VPD EEPROM	$A8	AT24C64 (8192x8)
U4	RTM	$AA	Reserved for RTM
U43	User EEPROM 1	$AC	AT24C512 (65536x8)
U45	User EEPROM 2	$AE	AT24C512 (65536x8)
U42	RTC	$D0	DS 1337 real-time clock
U6	IDT Clocking Chip	$DC	IDT ICS9FG108

Table 4-4 P2020 I2C Port2 Devices

Ref Designator	I2C Device	I2C 8-bit Base Address	Device Type
XJ2	XMC1	$A4	XMC dependent
Xj1	XMC2	$A6	XMC dependent

4.14 Reset/Control CPLD

The CPLD provides the following functions:

- Power control and fault detection
- Reset sequence and reset management
- Status and control registers
- Miscellaneous control logic
- Watchdog timer
- 32-bit Tick Timer
- Clock generator
- Switch decoder and LED controller

4.15 Power Management

The MVME2502 backplane is utilized to derive +3.3V, +2.5V, +1.8V, +1.5V, +1.2V, +1.05V voltage rail. Each voltage rail is controlled by the CPLD through an enable pin of the regulator, while the output is monitored through power good signal. If a voltage rail fails, the CPLD will disable all of the regulators. To restart the system, the chassis power switch must be power-cycled.

4.15.1 Onboard Voltage Supply Requirement

The onboard power supply is considered to be out of regulation if the output voltage level is below the minimum required power or goes beyond the maximum.

Table 4-5 Voltage Supply Requirement

	Voltage Rail Requirement	
Voltage Rail	Minimum	Maximum
+3.3 V	3.15 V	3.45 V
+2.5 V	2.375 V	2.625 V
+1.8 V	1.7 V	1.9 V

Table 4-5 Voltage Supply Requirement

Voltage Rail	Voltage Rail Requirement	
	Minimum	Maximum
+1.5 V	1.425 V	1.575 V
+1.2 V	1.14 V	1.26 V
+1.2 V_SW	1.14 V	1.26 V
+1.05 V	1.0 V	1.1 V

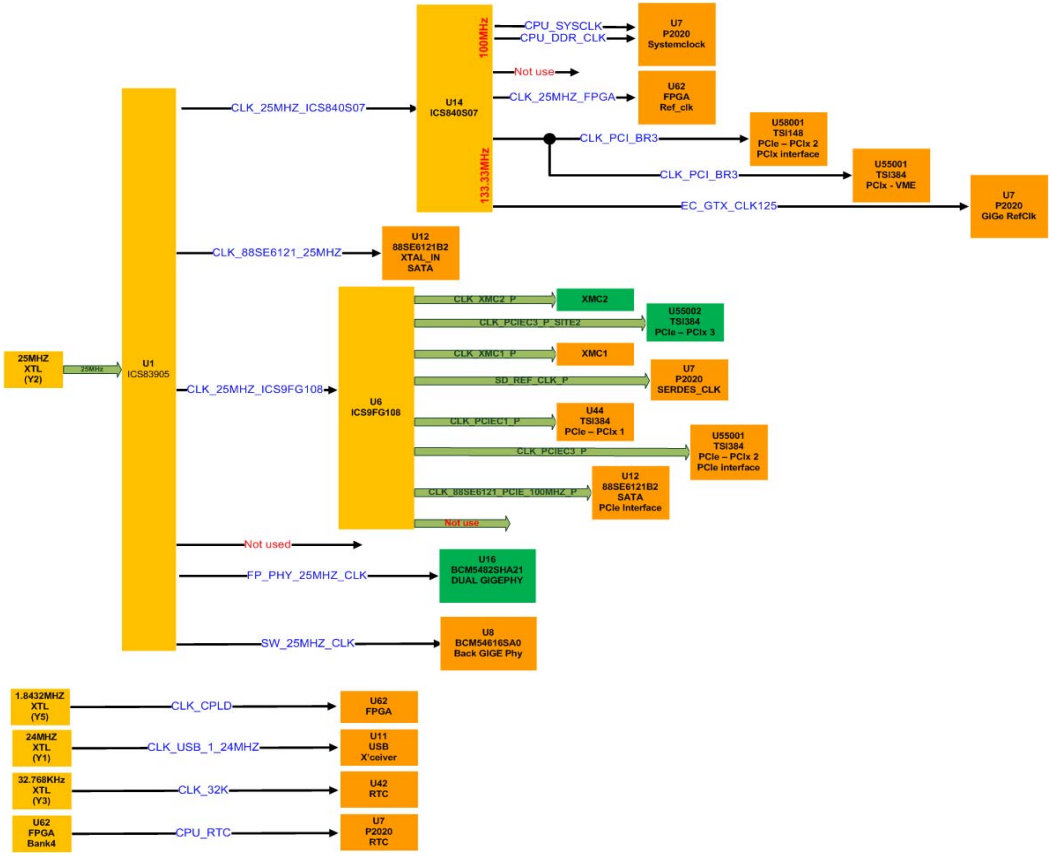
4.15.2 Power Up Sequencing Requirements

The power up sequence describes the voltage rail power up timing, which is designed to support all the chip supply voltage sequencing requirement.

4.16 Clock Structure

A total of three IDT chips, a discrete oscillator and crystal to support all the clock requirements of MVME2502.

Figure 4-3 Clock Distribution Diagram



4.17 Reset Structure

MVME2502 reset will initiate after the power up sequence if the 1.5 V power supply is "GOOD". When the board is at “ready” state, the reset logic will monitor the reset sources and implement the necessary reset function.

4.17.1 Reset Sequence

The timing of the reset sequence supports each chip reset requirements with respect to the power supply.

4.18 Thermal Management

The MVME2502 utilizes two on-board temperature sensors: one for the board and the other for the CPU temperature sensor. The board temperature sensor is located near the processor. The CPU temperature sensor is located on the processor.

The MVME2502 thermal management support will interrupt the process only to show the current board and CPU temperature. This interrupt is routed directly to one of the processor's IRQ4.

The table below shows the low and high threshold temperature in order for the interrupt to be asserted.

Table 4-6 Thermal Interrupt Threshold

Board Variant	Board Temperature Limit	Board Temperature Limit		CPU Temperature Limit	
		Low	High	Low	High
Standard Variant	0°C to +55°C	0°C	70°C	0°C	90°C
Extended Temperature Variant	-55°C to +71°C	-40°C	90°C	-40°C	100°C

4.19 Real-Time Clock Battery

The MVME2502 provides a through hole socket for a CR1225 48mAh lithium battery to provide backup power for the onboard RTC when primary power is unavailable.

4.20 Debugging Support

The following information shows the details of Artesyn debugging support as applied to the MVME2502.

4.20.1 POST Code Indicator

The following table shows the LED status of the POST Codes. For the location of the POST Code LEDs, see *Onboard LEDs, on page 46*.

Logic 1 means LED is "ON", Logic 2 means LED is "OFF"

Table 4-7 POST Code Indicator on the LED

Sequence	D33	D32	D35	Description
1	Off	Off	Off	U-boot has been copied from SPI flash to CPU cache.
2	Off	On	Off	Serial console has been initialized, some text is visible on the terminal.
3	Off	On	On	DDR has been initialized using SPD parameters, Execution is still in the cache.
4	On	Off	Off	Execution has been relocated to RAM.
5	On	Off	On	PCI has been initialized.
6	On	On	Off	POST routines are finished.
7	On	On	On	Additional SW routines are finished.
8	Off	Off	Off	U-boot prompt is visible on the terminal, can start loading OS image from USB, Ethernet, SATA SSD, SD.

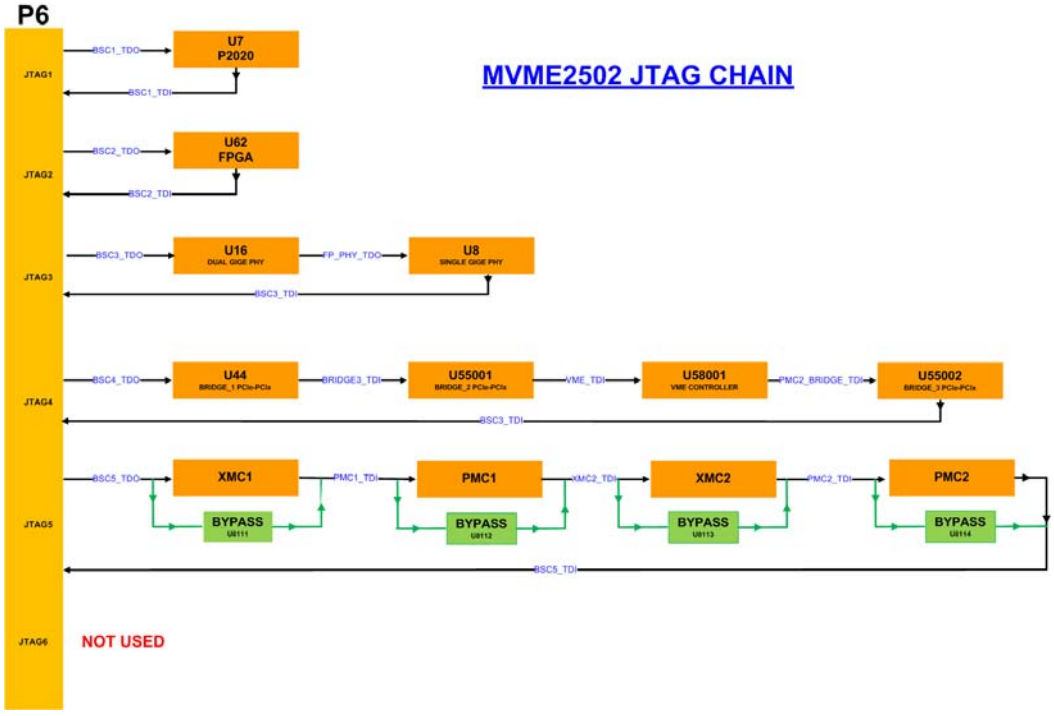
4.20.2 JTAG Chain and Board

The MVME2502 is designed to work with separate JTAG board rather than with an onboard JTAG multiplexer. The chip can support up to a 6-scan port and the board's boundary scan requires the following to function: ASSET hardware, JTAG board and JTAG cable. The MVME2502 provides a 60-pin header that can connect to the JTAG board via customize cable.

The JTAG bypass will connect when no XMC or PMC is connected to its corresponding locations. Once an external XMC or PMC is un-mounted its corresponding JTAG bypass will close, to complete the JTAG chain.

The JTAG board provides three different connectors for the ASSET hardware, flash programming and the MVME2502 JTAG connector. The board is equipped with TTL buffers to help improve the signal quality as it traverses over the wires.

Figure 4-4 JTAG Chain Diagram



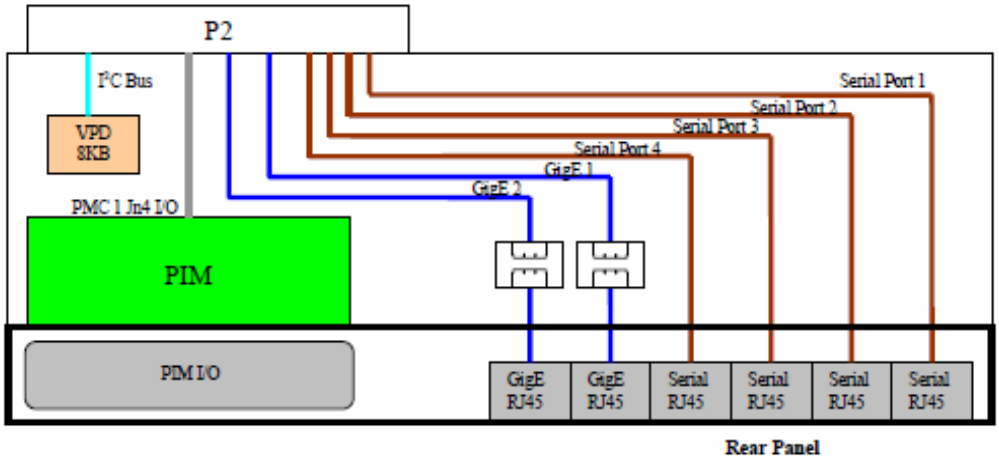
4.20.3 Custom Debugging

Custom debugging makes use of the common on-chip processor. Refer to *Common On-Chip Processor (COP), on page 74* for details.

4.21 Rear Transition Module (RTM)

The MVME2502 RTM Block diagram is illustrated below:

Figure 4-5 RTM Block Diagram



The MVME2502 is compatible with the MVME7216E RTM.

The MVME7216E RTM is for I/O routing through the rear of a compact VMEbus chassis. It connects directly to the VME backplane in chassis with an 80 mm deep rear transition area. It has the following features:

Table 4-8 Transition Module Features

Function	Features
I/O	• One five-row P2 backplane connector for serial and Ethernet I/O passed from the MVME2502. • Four RJ-45 connectors for rear panel I/O: four asynchronous serial channels. • Two RJ-45 connectors with integrated LEDs for rear panel I/O: two 10/100/1000 Ethernet channels. • One PIM site with rear panel I/O.

Memory Maps and Registers

5.1 Overview

System resources including system control and status registers, external timers, and the QUART are mapped into 16 MB address range accessible from the MVME2502 local bus through the P2020 QorIQ LBC.

5.2 Memory Map

The following table shows the physical address map of the MVME2502.

Table 5-1 Physical Address Map

Device Name	Start Address	End Address	Size
DDR	0x0000_0000	0x7fff_ffff	2 GB
PCIE 3 Mem	0x8000_0000	0x9fff_ffff	512 MB
PCIE 2 Mem	0xa000_0000	0xbfff_ffff	512 MB
PCIE 1 Mem	0xc000_0000	0xdfff_ffff	512 MB
PCIE 3 IO	0xffc0_0000	0xffc0_ffff	64 KB
PCIE 2 IO	0xffc1_0000	0xffc1_ffff	64 KB
PCIE 1 IO	0xffc2_0000	0xffc2_ffff	64 KB
UART0	0xffc4_0000	0xffc4_ffff	64 KB
UART1	0xffc5_0000	0xffc5_ffff	64 KB
UART2	0xffc6_0000	0xffc6_ffff	64 KB
UART3	0xffc7_0000	0xffc7_ffff	64 KB
Timer	0xffc8_0000	0xffc8_ffff	64 KB
CPLD	0xffdf_0000	0xffdf_0fff	4 KB
CCSR	0xffe0_0000	0xffef_ffff	1 MB
MRAM	0xfff0_0000	0xfff7_ffff	512 KB

5.3 Flash Memory Map

The table below lists the memory range designated to U-boot and ENV variables.

Table 5-2 Flash Memory Map

Description	Memory Area
U-boot	0x00000000 0x0008ffff
Reserved	0x00090000 0x0009ffff
ENV Variables	0x00100000 0x0011ffff
Available Flash	0x00120000 0x007fffff

5.4 Linux Devices Memory Map

The table below lists the memory ranges designated to different devices in Linux.

Table 5-3 Linux Devices Memory Map

Device Memory Range	Memory Area	Size
Ram Mem	0x00000000 0x7fffffff	2 GB
PCIE3 Mem	0x80000000 0x9fffffff	512 MB
PCIE2 Mem	0xa0000000 0xbfffffff	512 MB
PCIE1 Mem	0xc0000000 0xdfffffff	512 MB
MRAM	0xfff00000 0xfff7ffff	512 KB
PCIE3 IO	0xffc00000 0xffc0fff	64 KB
PCIE2 IO	0xffc10000 0xffc1ffff	64 KB
PCIE1 IO	0xffc20000 0xffc2ffff	64 KB
QUART0	0xffc40000 0xffc4ffff	64 KB
QUART1	0xffc50000 0xffc5ffff	64 KB
QUART2	0xffc60000 0xffc6ffff	64 KB
QUART3	0xffc70000 0xffc7ffff	64 KB
Timer	0xffc80000 0xffc8ffff	64 KB

Table 5-3 Linux Devices Memory Map

Device Memory Range	Memory Area	Size
CPLD	0xffdf0000 0xffdf0fff	4 KB
ecm local access window CCSR	0xffe00000 0xffe00ffff	4 KB
ecm (Error Correction Module) CCSR	0xffe01000 0xffe01fff	4 KB
Memory Controller CCSR	0xffe02000 0xffe02fff	4 KB
I2C1 CCSR	0xffe03000 0xffe030ff	256 B
I2C2 CCSR	0xffe03100 0xffe031ff	256 B
UART0 CCSR	0xffe04500 0xffe045ff	256 B
UART1CCSR	0xffe04600 0xffe046ff	256 B
ELBC CCSR	0xffe05000 0xffe05fff	4 KB
SPI CCSR	0xffe07000 0xffe07fff	4 KB
PCIE3 CCSR	0xffe08000 0xffe08fff	4 KB
PCIE2 CCSR	0xffe09000 0xffe09fff	4 KB
PCIE1CCSR	0xffe0a000 0xffe0afff	4 KB
DMA2 CCSR	0xffe0c100 0xffe0c303	516 B
GPIO CCSR	0xffe0fc00 0xffe0fcff	256 B
L2 Cache CCSR	0xffe20000 0xffe20fff	4 KB
DMA1 CCSR	0xffe21100 0xffe21303	516 B
USB CCSR	0xffe22000 0xffe22fff	4 KB
ETSEC1 CCSR	0xffe24000 0xffe24fff	4 KB
ETSEC2 CCSR	0xffe25000 0xffe25fff	4 KB
ETSEC3 CCSR	0xffe26000 0xffe26fff	4 KB
SDHCI CCSR	0xffe2e000 0xffe2efff	4 KB
Crypto CCSR	0xffe30000 0xffe3ffff	64 KB
msi CCSR	0xffe41600 0xffe4167f	128 B
mpic CCSR	0xffe40000 0xffe7ffff	256 KB
Global Utilities CCSR	0xffee0000 0xffee0fff	4 KB
L2 Cache Mem	0xf0f80000 0xf0ffffff	512 KB

5.5 Programmable Logic Device (PLD) Registers

5.5.1 PLD Revision Register

The MVME2502 provides a PLD revision register that can be read by the system software to determine the current version of the timers/registers PLD.

Table 5-4 PLD Revision Register

REG	PLD Revision Register - 0xFFDF0000							
Bit	7	6	5	4	3	2	1	0
Field	PLD Rev							
OPER	R							
RESET	(TBD)							

Field Description

PLD_REV	8-bit field containing the current timer/register PLD revision. The revision number starts at 01.

5.5.2 PLD Year Register

The MVME2502 PLD provides an 8-bit register which contains the build year of the timers/registers PLD.

Table 5-5 PLD Year Register

REG	PLD Year Register - 0xFFDF0004							
Bit	7	6	5	4	3	2	1	0
Field	PLD Rev							
OPER	R							
RESET	(TBD)							

5.5.3 PLD Month Register

The MVME2502 PLD provides an 8-bit register which contains the build month of the timers/registers PLD.

Table 5-6 PLD Month Register

REG	PLD Year Register - 0xFFDF0005							
Bit	7	6	5	4	3	2	1	0
Field	PLD Rev							
OPER	R							
RESET	(TBD)							

5.5.4 PLD Day Register

MVME2502 PLD provides an 8-bit register which contains the build day of the timers/registers PLD.

Table 5-7 PLD Day Register

REG	PLD Revision Register - 0xFFDF0006							
Bit	7	6	5	4	3	2	1	0
Field	PLD Rev							
OPER	R							
RESET	(TBD)							

5.5.5 PLD Sequence Register

The MVME2502 PLD provides an 8-bit register which contains the sequence of the PLD which is in synchrony with the PCB version.

Table 5-8 PLD Sequence Register

REG	PLD Revision Register - 0xFFDF0007							
Bit	7	6	5	4	3	2	1	0

Table 5-8 PLD Sequence Register

REG	PLD Revision Register - 0xFFDF0007							
Bit	7	6	5	4	3	2	1	0
Field	PLD Rev							
OPER	R							
RESET	(TBD)							

5.5.6 PLD Power Good Monitor Register

The MVME2502 PLD provides an 8-bit register which indicates the instantaneous status of the supply's power good signals.

Table 5-9 PLD Power Good Monitor Register

REG	PLD PWRDG_MNTR - 0xFFDF0012							
Bit	7	6	5	4	3	2	1	0
Field	RSVD	PWR_V1P05_PWRGD	PWR_V1P2_PWRGD	PWR_V1P8_PWRGD	PWR_V3P3_PWRGD	PWR_V2P5_PWRGD	PWR_V1P2_SW_PWRGD	PWR_V1P5_PWRGD
OPER	R							
RESET	0	0	0	0	0	0	0	0

Field Description

PWR_V1P05_PWRGD	1.05V Core supply power good indicator
PWR_V1P2_PWRGD	1.2V Supply power good indicator
PWR_V1P8_PWRGD	1.8V Supply power good indicator

PWR_V3P3_PWRGD	3.3V Supply power good indicator
PWR_V2P5_PWRGD	2.5V Supply power good indicator
PWR_V1P2_SW_PWRGD	1.2V SW Supply power good indicator
PWR_V1P5_PWRGD	1.5V Supply power good indicator 1 - Supply Good and Stable 0 - Otherwise

5.5.7 PLD LED Control Register

The MVME2502 PLD provides an 8-bit register which controls the eight LEDs.

Table 5-10 PLD LED Control Register

REG	PLD LED_CTRL - 0xFFDF001C							
Bit	7	6	5	4	3	2	1	0
Field	D1	D35	D34	D33	D38	D37	D2 Red	D2 Yellow
OPER	R/W							
RESET	1	0	0	0	0	0	0	0

1 - LED on

0 - LED off

For more information on LEDs, refer to Table "Front Panel LEDs" on page 44 and Table "Onboard LEDs Status" on page 46.

5.5.8 PLD PCI/PMC/XMC (Slot1) Monitor Register

The MVME2502 PLD provides an 8-bit register which indicates the status of the PCI/PMC/XMC interface signals.

Table 5-11 PLD PCI/PMC/XMC (Slot1) Monitor Register

REG	PLD PCI_PMC_XMC_MNTR - 0xFFDF001D							
Bit	7	6	5	4	3	2	1	0
Field	RSVD	RSVD	MUX1_SEL_SW	SW2-4	PMC1_EREADY	PMC1P_N	XMCP1_N	PCI1_PCIXCAP
OPER	R							
RESET	0	0	1	X	X	X	X	X

Field Description

MUX1_SEL_SW
Select for PCIe MUX1 (R/W)
1 - PMC
0 - XMC

SW2-4
SW2-4 state (User defined)
0 - SW2-4 closed
1 - SW2-4 open (default)

PMC1_EREADY
Indicates PCI device is ready for enumeration.
1 - PMC ready for enumeration
0 - PMC is not ready for enumeration

PMC1P_N
PMC Presence Indicator
1 - PMC is not present
0 - PMC is present

XMCP1_N
XMC Presence Indicator
1 - XMC is not present
0 - XMC is present

PCI1_PCIXCAP
PCI Capability Indicator
1 - PCI-X capable
0 - PCI capable

5.5.9 PLD PCI/PMC/XMC (Slot2) Monitor Register

The MVME2502 PLD provides an 8-bit register which indicates the status of the SATA/PMC/XMC interface signals.

Table 5-12 PLD PCI/PMC/XMC (Slot2) Monitor Register

REG	PLD PCI_PMC_XMC_MNTR - 0xFFDF001F							
Bit	7	6	5	4	3	2	1	0
Field	SD1_MUX_SEL1	SD1_MUX_SEL0	SW2-4	PMC2_EREADY	SATA0_DETECT_N	PMC2P_N	XMCP2_N	PMC2_PCIXCAP
OPER	R							
RESET	X	X	X	X	X	X	X	X

Field Description

SD1_MUX_SEL[1:0] Select for PCIe MUX1 (Read Only)
11 - XMC (default)
10 - PMC
01-SATA
00-Unused

SW2-4 SW2-4 state (User defined)
0 - SW2-4 closed
1 - SW2-4 open (default)

PMC2_EREADY Indicates PCI device is ready for enumeration.
1 - PMC ready for enumeration
0 - PMC is not ready for enumeration

SATA0_DETECT_N	SATA drive presence indicator 1-SATA not present 0-SATA present
PMC2P_N	PMC Presence Indicator 1 - PMC is not present 0 - PMC is present
XMCP2_N	XMC Presence Indicator 1 - XMC is not present 0 - XMC is present
PMC2_PCIXCAP	PCI Capability Indicator 1 - PCI-X capable 0 - PCI capable

5.5.10 PLD U-Boot and TSI Monitor Register

The MVME2502 PLD provides an 8-bit register which indicates the status of the U-Boot's normal environment switch and TSI interface signals.

Table 5-13 PLD U-Boot and TSI Monitor Register

REG	PLD PCI_PMC_XMC_MNTR - 0xFFDF001E							
Bit	7	6	5	4	3	2	1	0
Field	RSVD	RSVD	RSVD	RSVD	RSVD	BDFAIL_N	NORMAL_ENV	SCON
OPER	R							
RESET	0	0	0	0	0	X	X	X

Field Description

BDFAIL_N	TSI148 BDFAIL_N Pin out 1 - No TSI Fail 0 - TSI Fail
NORMAL_ENV	Normal Environment Switch Indicator 1 - Use safe ENV 0 - Use normal ENV
SCON	System Controller Indicator 1 - System Controller 0 - Non-system Controller

5.5.11 PLD Boot Bank Register

The MVME2502 PLD provides an 8-bit register which is used to declare successful U-Boot loading, indicating the SPI boot bank priority and actual SPI bank it booted from.

Table 5-14 PLD Boot Bank Register

REG	PLD Boot Bank - 0xFFDF0050							
Bit	7	6	5	4	3	2	1	0
Field	SPI_GOODReg (write 0xA4 into this reg to indicate successful loading of the U-Boot.						BOOT_BLOCK_A	BOOT_SPI
OPER	R/W						R	R
RESET	0	0	0	0	0	0	X	0

Field Description

BOOT_BLOCK_A	Boot Block Manual Selector Switch 1 - SPI0 0 - SPI1
BOOT_SPI	Actual Boot Bank 1 - SP1 0 - SPI0

5.5.12 PLD Write Protect and I2C Debug Register

The MVME2502 PLD provides an 8-bit register which is used to indicate the status of I2C and SPI write-protect manual switches and is used to control the SPI write-enable. I2C debug ports are also provided in this register which can be used in controlling the bus' status.

Table 5-15 PLD Write Protect and I2C Debug Register

REG	PLD Write Protect I2C Debug- 0xFFDF0054							
Bit	7	6	5	4	3	2	1	0
Field	RSVD	MASTER_WP_DISABLED	FLASH_WP_N	I2C_DEBUG_EN	SERIAL_FLASH_WP	RSVD	I2C_1_D	I2C_1_C
OPER	R	R	R	R/W	R/W	R	R/W	R/W
RESET	0	1	0	0	1	0	1	1

Field Description

SPD_WP-	SPD write-protection 0 - SPD Writesenabled 1 - SPD Writes disabled
MASTER_WP-	MASTER WP Switch (S2-6) 0-Switch S2-6 closed. SPI, SPD, VPD, USER FLASH writeable 1-Switch S2-6 open, register bits control write protection

USER_WP-	USER FLASH write-protect 1 - USER I2C FLASH writes disabled 0 - USER I2C FLASH writes enabled
I2C_DEBUG_EN	I2C debug ports (I2C_1_D and I2C_1_C) enable 1 - Drive Enabled 0 - Drive Disabled
SERIAL_FLASH_WP	SPI devices write-protect register 0 - SPI FLASH writes enabled 1 - SPI FLASH writes disabled
I2C_1_D	I2C debug port-Data 0 - Driven Low 1 - HiZ
I2C_1_C	I2C debug port-Clock 0 - Driven Low 1 - HiZ

When SERIAL_FLASH_WP is set to "Low", this port will automatically read as low due to "AND" connection between the two ports.

5.5.13 PLD Test Register 1

The MVME2502 PLD provides an 8-bit general purpose read/write register which can be used by the software for PLD testing or general status bit storage.

Table 5-16 PLD Test Register 1

REG	PLD Test Register 1- 0xFFDF0008							
Bit	7	6	5	4	3	2	1	0
Field	TEST_REG1							
OPER	R/W							

Table 5-16 PLD Test Register 1

REG	PLD Test Register 1- 0xFFDF0008
RESET	00

Field Description

TEST_REG1 General purpose 8-bit R/W field

5.5.14 PLD Test Register 2

The MVME2502 PLD provides an 8-bit general purpose read/write register which can be used by the software for PLD testing or general status bit storage.

Table 5-17 PLD Test Register 2

REG	PLD Test Register 2- 0xFFDF0009							
Bit	7	6	5	4	3	2	1	0
Field	TEST_REG2							
OPER	R/W							
RESET	00							

Field Description

TEST_REG2 General purpose 8-bit R/W field

5.5.15 PLD GPIO2 Interrupt Register

The Abort switch, Tick Timer 0, 1 and 2 interrupts are ORed together. The MVME2502 provides an interrupt register that the system software reads to determine which device the interrupt originated from. GPIO2 will be driven "low" if any of the interrupts asserts.

Table 5-18 PLD GPIO2 Interrupt Register

REG	PLD Write Protect I2C Debug- 0xFFDF0095							
Bit	7	6	5	4	3	2	1	0
Field	CPU_RTC_SEL	SW2-3	RSVD	RSVD	NMI	TICK0_INT	TICK1_INT	TICK2_INT
OPER	R							
RESET	0	0	X	0	0	0	0	0

Field Description

CPU_RTC_SEL — CPU RTC Input Select
0-1.824MHz (default)
1-SQW/INTB from DS1337 RTC

SW2-3 — SW2-3 state (User defined)
0-SW2-3 closed
1-SW2-3 open (default)

NMI	Abort switch interrupt if pressed less than three seconds. 1 - Interrupt enabled 0 - No Interrupt
TICK0_INT	Tick Timer 0 interrupt 1 - Interrupt enabled 0 - No Interrupt
TICK1_INT	Tick Timer 1 interrupt 1 - Interrupt enabled 0 - No Interrupt
TICK2_INT	Tick Timer 2 interrupt 1 - Interrupt enabled 0 - No Interrupt

5.5.16 PLD Shutdown and Reset Control and Reset Reason Register

The MVME2502 provides an 8-bit register to execute the shutdown and reset commands. The board's reset reason is also included in this register.

Table 5-19 PLD Shutdown and Reset Control and Reset Reason Register

REG	PLD Shutdown and Reset Reason- 0xFFDF00FF							
Bit	7	6	5	4	3	2	1	0
Field	RSVD	Shutdown	Soft_RST	Clear_Cause	CPU_RESET	WD_TIME OUT	LRSTO	Sft_RST
OPER	R	W	W	W	R			
RESET	0	0	0	0	X	X	X	X

Field Description

Shutdown	Board Shutdown Register 1 - Shutdown Enable 0 - Shutdown Disable

Note: If a board entered the shutdown state (by writing a '1' in this register), the chassis' power needs to be cycled to power up the board again.

Soft_RST	Board Soft Reset (self clearing) 1 - Execute soft reset 0 - No reset
Clear_Cause	Clear Reset Reason (self clearing) 1 - Clear Reason 0 - None
CPU_RESET	CPU_HRESET_REQ_L Reset Reason 1 - Reset is due to CPU_HRESET_REQ_L signal 0 -None
WD_TIMEOUT	Watchdog Timeout Reset Reason 1 - Reset is due to watchdog timing out 0 - None
LRSTO	TSI LRSTO Reset Reason 1 - Reset is due to LRSTO signal 0 - None
Sft_RST	Soft Reset - Reset Reason 1 - Reset is due to Soft_RST register being set, or the front panel switch being pressed more than three 0 - None

5.5.17 EMMC Reset Register

The MVME2502 provides a register for EMMC Reset.

Table 5-20 PLD Shutdown and Reset Control and Reset Reason Register

REG	EMMC Reset Register							
Bit	7	6	5	4	3	2	1	0
Field	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	EMMC_RST_N
OPER	R							R/W
RESET	0	0	0	0	X	X	X	X

Field Description

EMMC_RST_N	EMMC Reset Bit 1 - Reset is deasserted 0 - Reset is asserted (write 0 to reset EMMC)

5.5.18 PLD Watchdog Timer Refresh Register

The MVME2502 provides a watchdog timer refresh register.

Table 5-21 PLD Watchdog Timer Refresh Register

REG	PLD Watch Dog Timer Load - 0xFFC80600															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Field	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	Refresh							
OPER	R															
RESET	0000															

Field Description

Refresh	Counter Refresh. When the pattern 0x00DB is written, the watchdog counter will be reset to zero.

5.5.19 PLD Watchdog Control Register

The MVME2502 provides a watchdog control register.

Table 5-22 PLD Watchdog Control Register

REG	PLD Watch Dog Timer Load - 0xFFC80604															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Field	Watchdog_EN	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD
OPER	R/W	R														
RESET	0000															

Field Description

EN Enable. If cleared, the watchdog timer is disabled. If set, the watchdog timer is enabled.

5.5.20 PLD Watchdog Timer Count Register

The MVME2502 provides a watchdog timer count register.

Table 5-23 PLD Watchdog Timer Count Register

REG	PLD Watchdog Timer Count - 0xffc80606
Bit	15:0
Field	Count
OPER	R/W
RESET	0xEA60 (60secs)

Field Description

Count	Count. These bits define the watchdog timer count value. When the watchdog counter is enabled, it will count up from zero (reset value) with a 1 ms resolution until it reaches the COUNT value set by this register. Watchdog will generate a soft reset signal if it bites. Setting this register to 0xEA60 or 60,000 counts will provide a watchdog timeout of 60 seconds.

5.5.21 PLD Watchdog Timer Count Value Register

The MVME2502 provides a watchdog timer count value register.

Table 5-24 PLD Watchdog Timer Count Register

REG	PLD Watchdog Timer Count Value- 0xffc80608
Bit	15:0
Field	Count Value
OPER	R
RESET	0x0000

Field Description

Count Value	Count value. These bits indicate the current value of the watch dog counter.

5.6 External Timer Registers

The MVME2502 provides a set of tick timer registers to access the three external timers implemented in the timers/registers PLD. These registers are 32-bit and are word writable. The following sections describe the timer prescaler and control register:.

5.6.1 Prescaler Register

The prescaler adjust value is determined by this formula:

```
Prescaler Adjust = 256-(CLKIN/CLKOUT)
```

CLKIN is the input clock source in MHz, and CLKOUT is the desired output clock reference in MHz.

Table 5-25 Prescaler Register

REG	Prescaler Register - 0xFFC80100															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Field	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	Prescaler Register (8-bits)							
OPER	R/W															
RESET	0x00e7															

The prescaler provides the clock required by each of the three times. The tick timers require a 1 MHz clock input. The input clock to the prescaler is 25 MHz. The default value is set for 0x00E7, which gives a 1 MHz reference clock for a 25 MHz input clock source.

5.6.2 Control Registers

Table 5-26 Control Registers

REG	Tick Timer 0 Control Register - 0xFFC80202 Tick Timer 1 Control Register - 0xFFC80302 Tick Timer 2 Control Register - 0xFFC80402															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Field	RSVD	RSVD	RSVD	RSVD	RSVD	INTS	CINT	ENINT	OVF				RSVD	COVF	COC	ENC
OPER	R/W															
RESET	0x0000															

Field Description

ENC	Enable counter. When the bit is set, the counter increments. When the bit is cleared, the counter does not increment.
COC	Clear Counter on Compare. When the bit is set, the counter is reset to 0 when it compares with the compare register. When the bit is cleared the counter is not reset.
COVF	Clear Overflow Bits. The overflow counter is cleared when a 1 is written to this bit.
OVF	Overflow Bits are the output of the overflow counter. It increments each time the tick timer sends an interrupt to the local bus interrupter. The overflow counter can be cleared by writing a 1 to the COVF bit.
ENINT	Enable Interrupt. When the bit is set, the interrupt is enabled. When the bit is cleared, the interrupt is not enabled.
CINT	Clear Interrupt.
INTS	Interrupt Status.
RSVD	Reserved for future implementation.

5.6.3 Compare High and Low Word Registers

The tick timer counter is compared to the Compare Register. When the values are equal, the tick timer interrupt is asserted and the overflow counter increments. If the clear-on-compare mode is enable, the counter is also cleared. For periodic interrupts, this equation should be used to calculate the compare value for a specific period (T):

Compare register value=T (us)

When programming the tick timer for periodic interrupt, the counter should be cleared to zero by software and then enabled. If the counter does not initially start at zero, the time to the first interrupt may be longer or shorter than expected. Note that the rollover time for the counter is 71.6 minutes.

Since the processor is 16-bits and the tick timer is 32-bits, the compare register was split in half. Accessing the whole register will require two transactions.

Table 5-27 Compare High Word Registers

REG	Tick Timer 0 Compare Value High Word - 0xFFC80204 Tick Timer 1 Compare Value High Word - 0xFFC80304 Tick Timer 2 Compare Value High Word - 0xFFC80404														
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Field	TickTimer Compare Value High Word (16-bits)															
OPER	R/W															
RESET	0x0000															

Table 5-28 Compare Low Word Registers

REG	Tick Timer 0 Compare Value Low Word - 0xFFC80206 Tick Timer 1 Compare Value Low Word - 0xFFC80306 Tick Timer 2 Compare Value Low Word - 0xFFC80406														
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Field	TickTimer Compare Value Low Word (16-bits)															
OPER	R/W															
RESET	0x0000															

5.6.4 Counter High and Low Word Registers

When enabled, the tick timer counter register increments every microsecond. Software may read or write the counter at any time.

Table 5-29 Counter High Word Registers

REG	Tick Timer 0 Counter Value High Word - 0xFFC80208 Tick Timer 1 Counter Value High Word - 0xFFC80308 Tick Timer 2 Counter Value High Word - 0xFFC80408														
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

Table 5-29 Counter High Word Registers (continued)

REG	Tick Timer 0 Counter Value High Word - 0xFFC80208 Tick Timer 1 Counter Value High Word - 0xFFC80308 Tick Timer 2 Counter Value High Word - 0xFFC80408
Field	TickTimer Counter Value High Word (16-bits)
OPER	R/W
RESET	0x0000

Table 5-30 Counter Low Word Registers

REG	Tick Timer 0 Counter Value Low Word - 0xFFC8020A Tick Timer 1 Counter Value Low Word - 0xFFC8030A Tick Timer 2 Counter Value Low Word - 0xFFC8040A														
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Field	TickTimer Counter Value Low Word (16-bits)															
OPER	R/W															
RESET	0x0000															

Boot System

6.1 Overview

The MVME2502 uses Das U-Boot, a boot loader software based on the GNU Public License. It boots the blade and is the first software to be executed after the system is powered on.

Its main functions are:

- Initialize the hardware
- Pass boot parameters to the Linux kernel
- Start the Linux kernel
- Update Linux kernel and U-Boot images

This section describes U-Boot features and procedures that are specific to the MVME2502. For general information on U-Boot, see http://www.denx.de/wiki/UBoot/WebHome.

6.2 Accessing U-Boot

1. Connect the board to a computer with a serial interface connector and a terminal emulation software running on it. The serial connector of the board is found on the face plate.
2. Configure the terminal software to use the access parameters that are specified in U-Boot. By default, the access parameters are as follows:
   - Baud rate: 9600
   - PC ANSI
   - 8 data bits
   - No parity
   - 1 stop bit

These serial access parameters are the default values. These can be changed from within the U-Boot. For details, refer to the U-Boot documentation.

3. Boot the MVME2502.
4. When prompted, press the "h" key.

U-Boot aborts the boot sequence and enters into a command line interface mode.

Enter the command **`setenv bootdelay -1; saveenv`** to disable the U-Boot auto-boot feature and let the U-Boot directly enter the command line interface after the next reboot/power up.

6.3 Boot Options

6.3.1 Booting from a Network

In this mode, U-Boot downloads and boots the Linux kernel from an external TFTP server and mounts a root file system located on a network server.

1. Make sure that the `kernel, dtb,` and `ramdisk` are accessible to the board from the TFTP server.

2. Configure U-Boot environment variables:
```
setenv ipaddr <IP address of MVME2502>
setenv serverip <IP address of TFTP server>
setenv gatewayip <gateway IP>
setenv netmask <netmask>
setenv bootargs 'root=/dev/ram rw console=ttyS0,9600n8
ramdisk_size=700000 cache-sram-size=0x10000'
saveenv
```

3. Transfer the files through the TFTP from the server to the local memory.
```
tftp 1000000 <kernel_image>
tftp 2000000 <ramdisk>
tftp C00000 <kernel dtb>
```

4. Boot the Linux from the memory.
```
bootm 1000000 2000000 c00000
```

6.3.2 Booting from an Optional SATA Drive

1. Make sure that the `kernel, dtb,` and `ramdisk` are saved in the SATA drive with ext2 partition.
2. Configure U-Boot environment variable:
```
setenv File_uImage <kernel_image>
setenv File_dtp <kernel dtb>
setenv File_ramdisk <ramdisk>
saveenv
```
3. Copy the files from the SATA drive to the memory:
```
# option: scsi - interface, 0:1 - device 0 partition 1
ext2load scsi 0:1 1000000 $File_uImage
ext2load scsi 0:1 2000000 $File_ramdisk
ext2load scsi 0:1 c00000 $File_dtp
```
4. Boot the Linux in memory.
```
bootm 1000000 2000000 c00000
```

6.3.3 Booting from a USB Drive

1. Make sure that the `kernel, dtb`, and `ramdisk` are saved in the USB drive with FAT partition.
2. Configure the U-Boot environment variable:
```
setenv File_uImage <kernel_image>
setenv File_dtp <kernel dtb>
setenv File_ramdisk <ramdisk>
saveenv
```
3. Initialize USB drive:
```
usb start
```
4. Load the files from the USB drive to the memory:
```
# option: usb - interface, 0:1 - device 0 partition 1
fatload usb 0:1 1000000 $File_uImage
fatload usb 0:1 2000000 $File_ramdisk
fatload usb 0:1 c00000 $File_dtb
```
5. Boot the Linux in memory:
```
bootm 1000000 2000000 c00000
```

6.3.4 Booting from an SD Card

1. Make sure that the `kernel, dtb`, and `ramdisk` are saved in the SD card with FAT partition.
2. Configure the U-Boot environment variable:
```
setenv File_uImage <kernel_image>
setenv File_dtp <kernel dtb>
setenv File_ramdisk <ramdisk>
saveenv
```
3. Initialize SD card:
```
mmcinfo
```
4. Load the files from the SD card to the memory:
```
# option: mmc - interface, 0:1 - device 0 partition 1
fatload mmc 0:1 1000000 $File_uImage
fatload mmc 0:1 2000000 $File_ramdisk
fatload mmc 0:1 c00000 $File_dtp
```
5. Boot the Linux in memory:
```
bootm 1000000 2000000 c00000
```

6.3.5 Booting VxWorks Through the Network

In this mode, the U-Boot downloads and boots VxWorks from an external TFTP server.

1. Make sure that the VxWorks image is accessible by the board from the TFTP server.
2. Configure U-Boot environment variables:
```
setenv ipaddr <IP address of MVME2502>
setenv serverip <IP address of TFTP server>
setenv gatewayip <gateway IP>
setenv netmask <netmask>
setenv vxboot 'tftpboot $vxbootfile && setenv bootargs
$vxbootargs && bootvx'
setenv vxbootfile <VxWorks_image>
setenv vxbootargs 'motetsec(0,0)<IP address of TFTP
server>:VxWorks h=<IP address of TFTP server> e=<IP address of
MVME2502>:ffffff00 b=<unused IP> u=vxworks pw=vxworks f=0x80'
saveenv
```

3. TFTP the files from the server to local memory, then boot:
   `run vxboot`

6.4 Using the Persistent Memory Feature

Persistent memory means that the RAM's memory is not deleted during a reset. Power cycling, or by temporarily removing the power and then powering up the blade again, will delete the memory content. Persistent memory feature is enabled by default.

This feature can be useful in many situations, including:

- Analyzing kernel logs after a Linux kernel panic
- Defining a particular memory region for the persistent storage of application specific data

Analyzing Kernel Log Files after a Kernel Panic

When a board that is running the Linux OS indicates a kernel panic, issue a reset (through the face plate button, for example) to analyze the cause, then subsequently analyze kernel log files. The persistent memory feature keeps the log files available in the memory.

To analyze the kernel log files:

1. Issue a reset.
2. Connect to U-Boot. For more information, see *Accessing U-Boot* on page 119.
3. Enter the following command to obtain memory addresses of the kernel log files: `.locate_kernel_log (1)`
   The memory addresses of any found kernel log files will be displayed.
4. Enter the following command to display the kernel logfile at any of these memory addresses: `.printf (<memory address>)`

The persistent memory is useful in application-specific data storage. The standard U-Boot variable `pram` can be used to reserve a memory region at the end of the physical memory to prevent it from being overwritten. U-Boot reports less memory to the Linux kernel through the `mem` parameter, indicating that the operating system should not use it either.

For more information, see the U-Boot documentation.

6.5 MVME2502 Specific U-Boot Commands

Table 6-1 MVME2502 Specific U-Boot Commands

Command	Description
base	Print or set address offset
bdinfo	Print board info structure
boot	Boot default, i.e., run 'bootcmd'
bootd	Boot default, i.e., run 'bootcmd'
bootelf	Boot from an ELF image in memory
bootm	Boot application image from memory
bootp	Boot image through network using BOOTP/TFTP protocol
bootvx	Boot VxWorks from an ELF image
cmp	Memory compare
coninfo	Print console devices and information
cp	Memory copy
cpu	Multiprocessor CPU boot manipulation and release
crc32	Checksum calculation
date	Get/set/reset date & time
diags	Runs POST diags
echo	Echo args to console
exit	Exit script
ext2load	Load binary file from a Ext2 file system
ext2ls	List files in a directory (default /)
fatinfo	Print information about file system
fatload	Load binary file from a DOS file system
fatls	List files in a directory (default /)
fdt	Flattened device tree utility commands
go	Start application at address 'addr'

Table 6-1 MVME2502 Specific U-Boot Commands (continued)

Command	Description
help	Print online help
i2c	I2C sub-system
iminfo	Print header information for application image
imxtract	Extract a part of a multi-image
interrupts	Enable or disable interrupts
itest	Return true/false on integer compare
loadb	Load binary file over serial line (kermit mode)
loads	Load S-Record file over serial line
loady	Load binary file over serial line (ymodem mode)
loop	Infinite loop on address range
md	Memory display
memmap	Displays memory map
mii	MII utility commands
mm	Memory modify (auto-incrementing address)
mmc	MMC sub system
mmcinfo	Display MMC info
moninit	Reset nvram, serial#, and write monitor to SPI flash
mtest	Simple RAM read/write test
mw	Memory write (fill)
nfs	Boot image through network using NFS protocol
nm	Memory modify (constant address)
pci	List and access PCI Configuration Space
pci_info	Show information about devices on PCI bus
ping	Send ICMP ECHO_REQUEST to network host
printenv	Print environment variables
rarpboot	Boot image through network using RARP/TFTP protocol
reset	Perform RESET of the CPU

Table 6-1 MVME2502 Specific U-Boot Commands (continued)

Command	Description
run	Run commands in an environment variable
saveenv	Save environment variables to persistent storage
script	Run a ';' delimited, ';;' terminated list of commands
scsi	SCSI sub-system
scsiboot	Boot from SCSI device
setenv	Set environment variables
setexpr	Set environment variable as the result of eval expression
sf	SPI flash sub-system
showvar	Print local hushshell variables
sleep	Delay execution for some time
soft_reset	Soft reset the board
source	Run script from memory
test	Minimal test like /bin/sh
tftpboot	Boot image through network using TFTP protocol
tsi148	Initialize and configure Tundra Tsi148
usb	USB sub-system
usbboot	Boot from USB device
version	Print monitor version

6.6 Updating U-Boot

To update the U-Boot, place the image in the RAM (address 0x1000000 in this example) before copying it to the SPI flash.

The following procedure will replace the image in SPI bank 0:

1. Disable SPI write-protect in CPLD register Chapter 5, *PLD Write Protect and I2C Debug Register*.
2. Ensure FLASH_WP_N in SMT Configuration Switch (S2) is in the "OFF" position.

3. Select SPI flash # 0:
   ```
   sf probe 0
   ```
4. Erase 0x90000 bytes starting at SPI address 0:
   ```
   sf erase 0 0x90000
   ```
5. Write 0x90000 bytes from RAM address 0x1000000 starting at SPI address 0:
   ```
   sf write 0x1000000 0 0x90000
   ```

To replace the image in SPI bank 1, replace step 2 with Select SPI flash # 1:

```
sf probe 1
```

Programming Model

7.1 Overview

This chapter includes additional programming information for the MVME2502.

7.2 Reset Configuration

The MVME2502 supports the power-on reset (POR) pin sampling method for processor reset configuration. Each option and the corresponding default setting are described in the following table.

Table 7-1 POR Configuration Settings

	CONFIG	CONFIG PINS	CONFIG	SELECTION	REMARKS
1	CCB Config	LA[29:31]	000	41: CCB CLOCK-400 MHz	
2	DDR PLL Config	TSEC_1588_CLK_OUT TSEC_1588_PULSE_OUT1 TSEC_1588_PULSE_OUT2	001	8:1 DDR PLL-800 MHz	DDR rate is twice the value of the DDR controller frequency, which is then divided by two through the software.
3	Core 0 PLL	LBCTL, LALE LGPL2/LOE/LFRE	110	3:1 CORE CLOCK PLL (1200 MHz)	For 1200 MHz board configuration
			100	2:1 CORE CLOCK PLL (800 MHz)	For 800 MHz board configuration
4	Core 1 PLL	LWE0, UART_SOUT1	110	3:1 CORE CLOCK PLL (1200 MHz)	For 1200 MHz board configuration
			100	2:1 CORE CLOCK PLL (800 MHz)	For 800 MHz board configuration
5	CPU Boot Config	LA27, LA16	10	e500 core 0 is allowed to boot without waiting for configuration by an external master, while e500 core 1 is prevented from booting until configured by an external master or the other core.	

Table 7-1 POR Configuration Settings (continued)

	CONFIG	CONFIG PINS	CONFIG	SELECTION	REMARKS
6	Boot Sequence	LGPL3/LFWP, LGPL5	11	CFG_BOOT_SEQ[1:0] = BOOT SEQUENCE DISABLED	
7	Memory Debug Config	DMA2_DACK0	1	Debug information from the DDR SDRAM controller is driven on the MSPCID and MDVAL signs (default)	
8	DDR Debug Config	DMA2_DDONE0	1	Debug information is not driven on ECC pins. ECC function in their normal mode (default).	
9	ELBCECC Enable Config	MSRCID0	0	Default operation: eLBC ECC checking is disabled	
10	Platform Speed	LA23	1	CFG_PLAT_SPEED:1=CCB CLOCK > = 333 MHz	
11	CORE 0 Speed	LA24	1	CFG_CORE0_SPEED:1=CORE FREQ>= 1000 MHz	For 1200 MHz board configuration
12			0	CFG_CORE0_SPEED:0=CORE FREQ<=1000 MHz	For 800 MHz board configuration
13	CORE 1 Speed	LA26	1	CFG_CORE1_SPEED:1=CORE FREQ>=1000 MHz	For 1200 MHz board configuration
14			0	CFG_CORE1_SPEED:0=CORE FREQ<=1000 MHz	For 800 MHz board configuration
15	DDR Controller Speed	LA26	1	CFG_DDR_SPEED:1=DDR FREQ>= 500 MHz	
16	Engineering use	LA[22:20] UART_SOUT[0], TRIG_OUT, MSRCID[1], MSRCID[4], DMA1_DDONE_B[0]	111111 11	Default (for future use)	
17	SerDes Ref Clock Config	TSEC_1588_ALARM_OUT1	1	SerDes expects a 100 MHz reference clock frequency (default).	

Table 7-1 POR Configuration Settings (continued)

	CONFIG	CONFIG PINS	CONFIG	SELECTION	REMARKS
18	ETSEC2 SGMII Mode	LGPL1	1	eTSEC2 Ethernet interface operates in standard parallel interface mode and uses the TSEC_2'pins (default).	
19	ETSEC3 SGMMI Mode	TSEC_1588_ALARM _OUT2	1	eTSEC3 Ethernet interface operates in standard parallel interface mode and uses the TSEC_3'pins (default).	
20	ETSEC1 and ETSEC2 Width	EC_MDC	0	eTSEC1 and eTSEC2 Ethernet interfaces operate in reduced pin mode (either RTBI, RGMI, RMII or 8-bit FIFO mode).	
21	ETSEC1 Protocol	TSEC1_TXD0, TSEC1_TXD7	10	The eTSEC2 controller operates using the GMII protocol (or RGMII, if configured in reduced mode) if its not configured to operate in SGMII mode.	
22	ETSEC2 Protocol	TSEC2_TXD0, TSEC2_TXD7	10	The eTSEC2 controller operates using the GMII protocol (or RGMII, if configured in reduced mode) if its not configured to operate in SGMII mode.	
23	ETSEC3 Protocol	UART_RTS0, UART_RTS1	10	The eTSEC3 controller operates using the RGMII protocol if not configured to operate in SGMII mode.	

Table 7-1 POR Configuration Settings (continued)

	CONFIG	CONFIG PINS	CONFIG	SELECTION	REMARKS
24	BOOT ROM Location	TSEC1_TXD[6:4], TSEC1_TX_ER	011X	On-chip boot ROM-SPI configuration (x=0), SDHC (x=1)	
25	Host/Agent Config	LWE1/LBS1, LA[18:19]	111	The processor acts as the host/root complex for all PCI-E/Serial Rapid IO interfaces (default).	
26	I/O Port Select	TSEC1_TXD[3:1], TSEC2_TX_ER	0010	PCI-E 1 (x1) (2.5 Gbps) - SerDes lane 0 PCI-E 2 (x1) (2.5 Gbps) - SerDes lane 2 PCI-E 3 (x2) (2.5 Gbps) - SerDes lane 2-3	
27	DDR SDRAM TYPE	TSEC2_TXD1	1	DDR31.5 V. CKE low at reset (default)	
28	SerDes PLL Time Out Enable	TRIG_OUT	1	Disable PLL lock time-out counter. The power-on-reset sequence waits indefinitely for the SerDes PLL to lock (default).	
29	System Speed	LA[28]	1	SYSCLOCK is above 66 MHz	
30	SDHC Card Detect Polarity	TSEC2_TXD_5	1	Not Inverted	
31	RAPID System Size			Default	RapidIO is not used

7.3 Interrupt Controller

The MVME2502 uses the MPC8548E integrated programmable interrupt controller (PIC) to manage locally generated interrupts. Currently defined external interrupting devices and interrupt assignments, along with corresponding edge/levels and polarities, are shown in the following table.

Table 7-2 MVME2502 Interrupt List

Interrupt Line	Interrupt Usage (Schematic)	Interface to CPU	Description
IRQ0	None		Reserved for VME interrupt
IRQ1	QUART_IRQ1	LBC	RTB Quart Interrupt
IRQ2	QUART_IRQ2	LBC	RTB Quart Interrupt
IRQ3	QUART_IRQ3	LBC	RTB Quart Interrupt
IRQ4	Temperature Interrupt	I2C	Two onboard Thermal Sensors: one is for CPU temp and the other is for board temp
IRQ5	Ethernet 1	Management I2C	Ethernet interrupt is handled by PHY/ Connected for flexibility
IRQ6	Ethernet 3	Management I2C	Ethernet interrupt is handled by PHY/ Connected for flexibility
IRQ7/ GPIO0	Ethernet 2	Management I2C	Ethernet interrupt is handled by PHY/ Connected for flexibility
IRQ8/ GPIO1	RTC (Real Time Clock)	12C	DS1337 INT_A
IRQ9/ GPIO2	CPLD Interrupt	LBC	NMI and 3 Tick Timer Interrupts
IRQ10// GPIO3	CPLD Interrupt	LBC	Not used
IRQ11// GPIO4	QUART_IRQ0	LBC	RTB Quart Interrupt

7.4 I2C Bus Device Addressing

The following table contains the I2C devices used for the MVME2502 and its assigned device address.

Table 7-3 I2C Bus Device Addressing

I2C Bus Address	Device Function	Size	Notes
0x50	SPD	256 x 8	
0x4C	ADT 7461 Temperature Sensor	N/A	
0x68	DS 1375 real-time clock	N/A	
0x54	VPD	8192 x 8	1
0x52	User configuration	65536 x 8	1
0x53	User configuration	65536 x 8	1
0x55	RTM EEPROM	8192 X 8	1, 2
0x56	XMC EEPROM	N/A	3

1. This is a dual address serial EEPROM.
2. The RTM Bus address can be manually changed through the S1 Switch on RTM. The default switch configuration will set the address to 0x55. Make sure that the address is unique to the RTM Bus address when setting the switch.
3. The address of the XMC EEPROM is configured through Geographic Address resistor on board.

7.5 Ethernet PHY Address

The assigned Ethernet PHY on the MII management bus is shown in the following table.

Table 7-4 PHY Types and MII Management Bus Address

Ethernet Port	Function / Location	PHY Types	PHY MIIM Address
TSEC1	Gigabit Ethernet port routed to front panel	BCM54616	1

Table 7-4 PHY Types and MII Management Bus Address

Ethernet Port	Function / Location	PHY Types	PHY MIIM Address
TSEC2	Gigabit Ethernet port routed to front or back panel, set by GBE_MUX_SEL in S2	BCM54616	7
TSEC3	Gigabit Ethernet port routed to back panel	BCM54616	3

7.6 Other Software Considerations

The following sections provide programming information in relation to various board components:

7.6.1 MRAM

The MVME2502 provides 512 K bytes of fast, non-volatile storage in the form of Magnetoresistive Random Access Memory (MRAM). The MRAM is directly accessible by software using processor load and store instructions similar to the DRAM. The difference is that the MRAM retains its contents even if the board is power cycled. The MRAM is accessed through the LBC.

7.6.2 Real Time Clock

The MVME2502 provides a battery backed-up DS1375 Real Time Clock (RTC) chip. The RTC chip provides time keeping and alarm interrupts. It is an I2C device and is accessed through the I2C bus address at 0x68.

7.6.3 Quad UART

The MVME2502 console RS232 port is driven by the UART built into the P2020 QorIQ chip. Additionally, the MVME2502 has a Quad UART chip which provides four additional 16550 compatible UART. These additional UART are internally accessed through the LBC bus. The Quad UART chip clock input (which is internally divided to generate the baud rate) is 1.8432 MHz. The four UART physically connect to RS232 DB9 serial ports through the RTM.

7.6.4 LBC Timing Parameters

The following table defines the timing parameters for the devices on the local bus.

Table 7-5 LBC Timing Parameters

	0 MRAM	1 UART 0	2 UART 1	3 UART 2	4 UART 3	5 CPLD	6 Timers
BCTLD	0	0	0	0	0	0	0
CSNT	1	1	1	1	1	1	1
ACS	10	10	10	10	10	10	10
XACS	0	0	0	0	0	0	0
SCY	0011	0011	0011	0011	0011	0011	0011
SETA	0	0	0	0	0	0	0
TRLX	0	0	0	0	0	0	0
EHTR	0	0	0	0	0	0	0
EAD	0	0	0	0	0	0	0

Field Description

BCTLD	Buffer control disable. 0 - LBCTL is asserted upon access to the current memory bank.
CSNT	Chip Select negation time. 1 - LCSn and LWE are negated one quarter of the bus clock cycle earlier
ACS	Address to chip-select setup. 10 - LCSn is outputted one quarter bus clock cycle after the address lines.
XACS	Extra Address to chip-select setup 0 - Address to chip-select setup is determined by ORx[ACS]
SCY	Cycle length in bus clocks 0011 - bus clock cycle wait state

SETA	External address termination 0 - Access is terminated internally by the memory controller unless the external device asserts LGTA earlier to terminate the access.
TRLX	Timing Relaxed 0 - Normal timing is generated by the GPCM.
EHTR	Extended hold time on read accesses. 0 - The memory controller generates normal timing. No additional cycles are inserted
EAD	External address latch delay 0 - No additional bus clock cycles (LALE asserted for one bus clock cycle only)

7.7 Clock Distribution

The clock function generates and distributes all of the clocks required for system operation. The ICS9FG108 is used to generate all the required PCI-E clocks. The 25 MHz clocks for the Ethernet PHY and SATA bridge are supplied by ICS83905. Most of the QorIQ P2020 clocks are generated by ICS840S07I chip. Additional clocks required by individual devices are generated near the devices using individual oscillators. The following table lists the clocks required on the MVME2502 along with the frequency and source.

Table 7-6 Clock Distribution

Device	Clock Signal	Frequency	Clock Tree Source	VIO
QorIQ P2020	CPU_SYSCLK	100MHz	ICS840S07I	+3.3V
QorIQ P2020	CPU_DDR_CLK	100MHz	ICS840S07I	+3.3V
QorIQ P2020	CLK_PCI_BR3	133Mhz	ICS840S07I	+3.3V
QorIQ P2020	EC_GTX_CLK125	125Mhz	ICS840S07I	+3.3V
ICS840S07I	CLK_25MHZ_ICS840S07	25Mhz	ICS83905AGILF	+3.3V
88SE9125	CLK_88SE9125_25MHZ	25Mhz	ICS83905AGILF	+3.3V
ICS9FG108	CLK_25MHZ_ICS9FG108	25Mhz	ICS83905AGILF	+3.3V
BCM54616S	BP_PHY_25MHZ_CLK	25Mhz	ICS83905AGILF	+3.3V
BCM54616S	FP_PHY_25MHZ_CLK	25Mhz	ICS83905AGILF	+3.3V

Table 7-6 Clock Distribution (continued)

Device	Clock Signal	Frequency	Clock Tree Source	VIO
BCM54616S	SW_25MHZ_CLK	25Mhz	ICS83905AGILF	+3.3V
XMC	CLK_XMC1	100MHz	ICS9FG108	DIFF
QorIQ P2020	SD_REF_CLK	100MHz	ICS9FG109	DIFF
TSI384	CLK_PCIEC1	100MHz	ICS9FG110	DIFF
TSI384	CLK_PCIEC3	100MHz	ICS9FG111	DIFF
88SE9125	CLK_88SE9125_PCIE_100MHZ	100MHz	ICS9FG112	DIFF
CPLD	CLK_CPLD	1.8432MHz	Oscillator	+3.3V
USB	CLK_USB_1_24MHZ	24MHz	Oscillator	+3.3V
QorIQ P2020	CPU_RTC	1MHz	CPLD	+3.3V
PMC	CLK_PMC1	33/66/100/133Mhz	TSI384	+3.3V
TSI148	CLK_PCI_BR3	133Mhz	ICS840S07I	+3.3V
RTC	CLK_32K	32.768KHz	DS32KHz	+3.3V
CPLD	CPU_LCK0	25MHz	QorIQ P2020	+3.3V
QUART	CLK_QUART	1.8432MHz	CPLD	+3.3V
ICS83905	CLK_25MHZ_ICS9FG108	25Mhz	ICS83905AGILF	+3.3V

7.7.1 System Clock

The system and DDR clock is driven by ICS840S07I. The following table defines the clock frequency.

Table 7-7 System Clock

SYSCLK	CORE	CCB Clock (Platform)	DDR3	LBC
100MHz	800/1200 MHz	400 MHz	400MHz	25MHz

7.7.2 Real Time Clock Input

The RTC clock input is driven by a 1 MHz clock generated by the CPLD. This provides a fixed clock reference for the QorIQ P2020 PIC timers which the software can use as a known time reference.

7.7.3 Local Bus Controller Clock Divisor

The local bus controller (LBC) clock output is connected to the CPLD for LBC bus transaction. It is also the source of 1 MHz (CPU_RTC) and CPLD tick timers.

A.1 Replacing the Battery

The figure below shows the location of the board battery.

Figure A-1 Battery Location ENP1 Variant

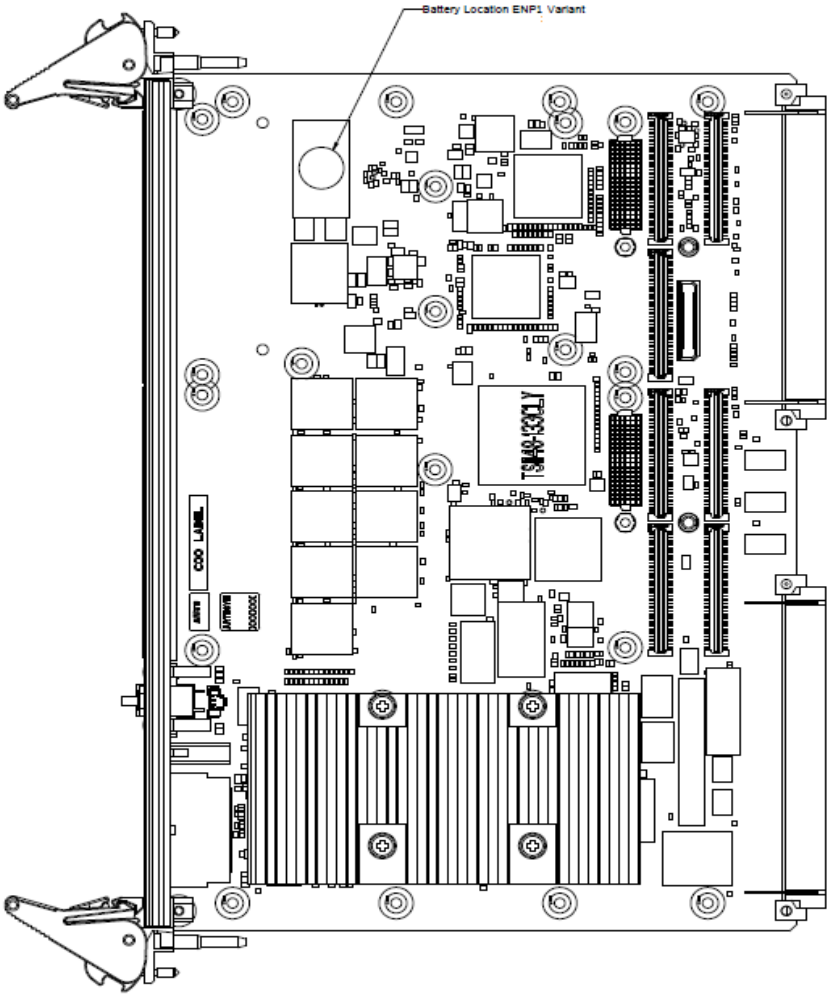
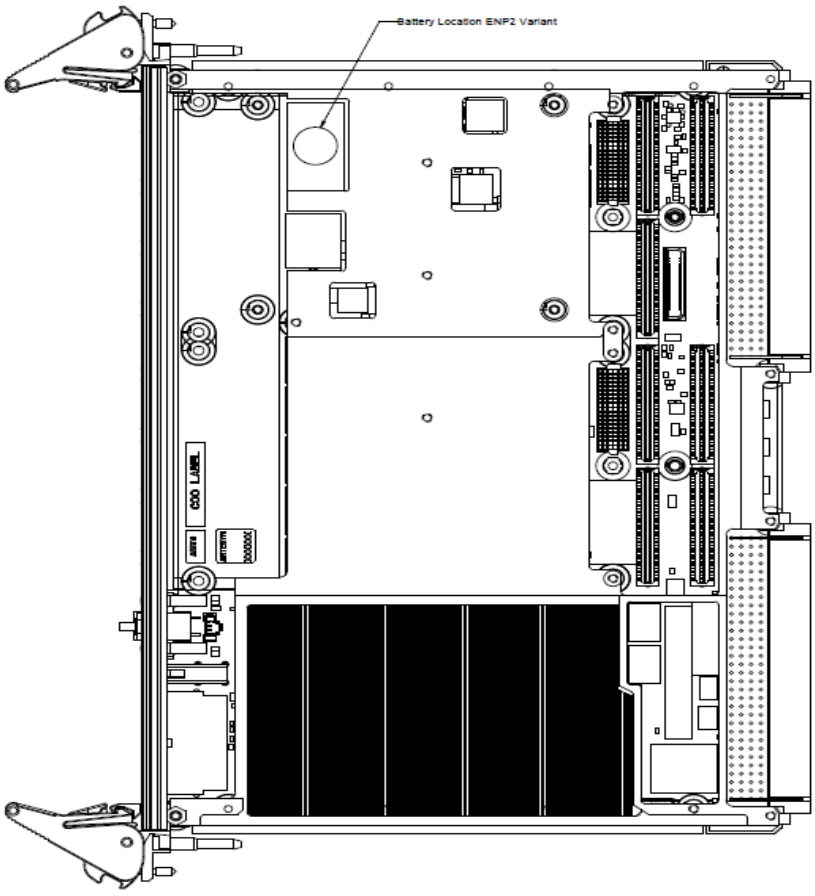


Figure A-2 Battery Location ENP2 Variant



The battery provides seven years of data retention, summing up all periods of actual data use. Artesyn Embedded Technologies therefore assumes that there is usually no need to replace the battery except, for example, in case of long-term spare part handling.

NOTICE

Board/System Damage

- Incorrect replacement of lithium batteries can result in a hazardous explosion.
- When replacing the on-board lithium battery, make sure that the new and the old battery are exactly the same battery models.
- If the respective battery model is not available, contact your local Artesyn sales representative for the availability of alternative, officially approved battery models.

Data Loss

- Replacing the battery can result in loss of time settings. Backup power prevents the loss of data during replacement.
- Quickly replacing the battery may save time settings.

Data Loss

- If the battery has low or insufficient power the RTC is initialized.
- Replace the battery before seven years of actual battery use have elapsed.

PCB and Battery Holder Damage

- Removing the battery with a screw driver may damage the PCB or the battery holder. To prevent damage, do not use a screw driver to remove the battery from its holder.

Replacement Procedure

To replace the battery, proceed as follows:

1. Remove the old battery.
2. Install the new battery with the plus sign (+) facing up.
3. Dispose of the old battery according to your country's legislation and in an environmentally safe way.

Related Documentation

B.1 Artesyn Embedded Technologies - Embedded Computing Documentation

The publications listed below are referenced in this manual. You can obtain electronic copies of Artesyn Embedded Technologies - Embedded Computing publications by contacting your local Artesyn sales office. For released products, you can also visit our Web site for the latest copies of our product documentation.

1. Go to www.artesyn.com/computing.
2. Under SUPPORT, click TECHNICAL DOCUMENTATION.
3. Under FILTER OPTIONS, click the Document types drop-down list box to select the type of document you are looking for.
4. In the Search text box, type the product name and click GO.

Table B-1 Artesyn Embedded Technologies - Embedded Computing Publications

Document Title	Publication Number
MVME2502 Data sheet	MVME2502-D3
MVME2502 Release Notes	6806800S46B
MVME2502 Quick Start Guide	6806800S32B
MVME2502 Safety Notes	6806800S33A
MVME7216 RTM Installation and Use	6806800M42C
MVME7216 RTM Quick Start Guide	6806800M53A
MVME7216 RTM Safety Notes	6806800M54A

B.2 Manufacturers' Documents

For additional information, refer to the following table for manufacturers' data sheets or user manuals. As an additional help, a source for the listed document is provided. Please note that while these sources have been verified, the information is subject to change without notice.

Table B-2 Manufacturers' Publications

Company	Document
Freescale	Freescale Semiconductor, QorIQ™ P2020 Integrated Processor Reference Manual, Rev. 0
Tundra Semiconductor Corporation	Tsi148™ PCI/X-to-VME Bus Bridge User Manual, March 2009

B.3 Related Specifications

For additional information, refer to the following table for related specifications. As an additional help, a source for the listed document is provided. Please note that, while these sources have been verified, the information is subject to change without notice.

Table B-3 Related Specifications

Organization	Document
American National Standards Institute (ANSI) VITA Standards Organization	ANSI/VITA 1.0-1994 (R2002), VME64 Standard
	ANSI/VITA 1.1-1997 (R2003), VME64x Extensions
	ANSI/VITA 1.5-2003, VME 2eSST
	ANSI/VITA 35-2000, Pin Assignments for PMC P4 Connector
	ANSI/VITA 39-2003, PCI-X for PMC and Processor PMC
VITA Standards Organization	XMC - High Speed, Switched Interconnect Protocols on PMC VITA 42.0 - 2005
	XMC General Purpose I/O Standard VITA 42.10
	XMC PCI Express Protocol Layer Standard VITA 42.3 - 2006

Table B-3 Related Specifications

Organization	Document
IEEE	IEEE 802.3 LAN/MAN CSMA/CD Access Method IEEE 802.3-2005
	IEEE Standard for a Common Mezzanine Card (CMC) Family IEEE Std 1386-2001
	IEEE Standard Physical and Environmental Layers for PCI Mezzanine Cards (PMC) IEEE Std 1386.1-2001
	IEEE Standard Test Access Port and Boundary-Scan Architecture IEEE Std 1149.1-2001
	Low Pin Count Interface Specification (LPC) Revision 1.1
Peripheral Component Interconnect Special Interest Group (PCI-SIG)	PCI Express Base Specification Revision 2.0
	PCI Local Bus Specification PCI Rev 3.0
	PCI-X Electrical and Mechanical Addendum to the PCI Local Bus Specification (PCI-X EM) Revision 2.0a
	PCI-X Protocol Addendum to the PCI Local Bus Specification (PCI-X PT) Revision 2.0a
Serial ATA International Organization (SATA-IO)	Serial ATA (SATA) Specification Revision 2.6
	Serial ATA II: Extensions to Serial ATA 1.0 Revision 1.0
Trusted Computing Group (TCG)	TPM Specification 1.2, Level 2 Revision 103 Version 1.2
USB Implementers Forum (USB-IF)	Universal Serial Bus Specification (USB) Revision 2.0

Safety Notes

This section provides warnings that precede potentially dangerous procedures throughout this manual. Instructions contained in the warnings must be followed during all phases of operation, service, and repair of this equipment. You should also employ all other safety precautions necessary for the operation of the equipment in your operating environment. Failure to comply with these precautions or with specific warnings elsewhere in this manual could result in personal injury or damage to the equipment.

Artesyn intends to provide all necessary information to install and handle the product in this manual. Because of the complexity of this product and its various uses, we do not guarantee that the given information is complete. If you need additional information, ask your Artesyn representative.

This product is a Safety Extra Low Voltage (SELV) device designed to meet the EN60950-1 requirements for Information Technology Equipment. The use of the product in any other application may require safety evaluation specific to that application.

Only personnel trained by Artesyn or persons qualified in electronics or electrical engineering are authorized to install, remove or maintain the product.

The information given in this manual is meant to complete the knowledge of a specialist and must not be used as replacement for qualified personnel.

Keep away from live circuits inside the equipment. Operating personnel must not remove equipment covers. Only Factory Authorized Service Personnel or other qualified service personnel may remove equipment covers for internal subassembly or component replacement or any internal adjustment.

Do not install substitute parts or perform any unauthorized modification of the equipment or the warranty may be voided. Contact your local Artesyn representative for service and repair to make sure that all safety features are maintained.

EMC (Results below)

This equipment has been tested and found to comply with the limits for a Class A digital device, pursuant to Part 15 of the FCC Rules. These limits are designed to provide reasonable protection against harmful interference when the equipment is operated in a commercial environment. This equipment generates, uses, and can radiate radio frequency energy and, if not installed and used in accordance with the instruction manual, may cause harmful interference to radio communications.

Operation of this equipment in a residential area is likely to cause harmful interference in which case the user will be required to correct the interference at his own expense. Changes or modifications not expressly approved by Artesyn Embedded Technologies Embedded Technologies could void the user's authority to operate the equipment. Board products are tested in a representative system to show compliance with the above mentioned requirements. A proper installation in a compliant system will maintain the required performance. Use only shielded cables when connecting peripherals to assure that appropriate radio frequency emissions compliance is maintained.

Operation

Product Damage
High humidity and condensation on the board surface causes short circuits.
Do not operate the board outside the specified environmental limits.
Make sure the board is completely dry and there is no moisture on any surface before applying power.

Damage of Circuits
Electrostatic discharge and incorrect installation and removal can damage circuits or shorten its life.
Before touching the board or electronic components, make sure that you are working in an ESD-safe environment.

Board Malfunction
Switches marked as “reserved” might carry production-related functions and can cause the board to malfunction if their setting is changed.
Do not change settings of switches marked as “reserved”. The setting of switches which are not marked as “reserved” has to be checked and changed before board installation.

Installation

Data Loss
Powering down or removing a board before the operating system or other software running on the board has been properly shut down may cause corruption of data or file systems.

Make sure all software is completely shut down before removing power from the board or removing the board from the chassis.

Product Damage
Only use injector handles for board insertion to avoid damage to the front panel and/or PCB. Deformation of the front panel can cause an electrical short or other board malfunction.

Product Damage
Inserting or removing modules with power applied may result in damage to module components.
Before installing or removing additional devices or modules, read the documentation that came with the product.

Cabling and Connectors

Product Damage
RJ-45 connectors on modules are either twisted-pair Ethernet (TPE) or E1/T1/J1 network interfaces. Connecting an E1/T1/J1 line to an Ethernet connector may damage your system.

- Make sure that TPE connectors near your working area are clearly marked as network connectors.
- Verify that the length of an electric cable connected to a TPE bushing does not exceed 100 meters.
- Make sure the TPE bushing of the system is connected only to safety extra low voltage circuits (SELV circuits).

If in doubt, ask your system administrator.

Battery

Board/System Damage
Incorrect exchange of lithium batteries can result in a hazardous explosion.
When exchanging the on-board lithium battery, make sure that the new and the old battery are exactly the same battery models.
If the respective battery model is not available, contact your local Artesyn sales representative for the availability of alternative, officially approved battery models.

Data Loss
Exchanging the battery can result in loss of time settings. Backup power prevents the loss of data during exchange.
Quickly replacing the battery may save time settings.

Data Loss
If the battery has low or insufficient power the RTC is initialized.
Exchange the battery before seven years of actual battery use have elapsed.

PCB and Battery Holder Damage
Removing the battery with a screw driver may damage the PCB or the battery holder. To prevent damage, do not use a screw driver to remove the battery from its holder.

Sicherheitshinweise

Dieses Kapitel enthält Hinweise, die potentiell gefährlichen Prozeduren innerhalb dieses Handbuchs vorrangestellt sind. Beachten Sie unbedingt in allen Phasen des Betriebs, der Wartung und der Reparatur des Systems die Anweisungen, die diesen Hinweisen enthalten sind. Sie sollten außerdem alle anderen Vorsichtsmaßnahmen treffen, die für den Betrieb des Produktes innerhalb Ihrer Betriebsumgebung notwendig sind. Wenn Sie diese Vorsichtsmaßnahmen oder Sicherheitshinweise, die an anderer Stelle diese Handbuchs enthalten sind, nicht beachten, kann das Verletzungen oder Schäden am Produkt zur Folge haben.

Artesyn Embedded Technologies ist darauf bedacht, alle notwendigen Informationen zum Einbau und zum Umgang mit dem Produkt in diesem Handbuch bereit zu stellen. Da es sich jedoch um ein komplexes Produkt mit vielfältigen Einsatzmöglichkeiten handelt, können wir die Vollständigkeit der im Handbuch enthaltenen Informationen nicht garantieren. Falls Sie weitere Informationen benötigen sollten, wenden Sie sich bitte an die für Sie zuständige Geschäftsstelle von Artesyn Embedded Technologies.

Das Produkt wurde entwickelt, um die Sicherheitsanforderungen für SELV Geräte nach der Norm EN 60950-1 für informationstechnische Einrichtungen zu erfüllen. Die Verwendung des Produkts in einer anderen Anwendung erfordert eine Sicherheitsüberprüfung für diese spezifische Anwendung.

Einbau, Wartung und Betrieb dürfen nur von durch Artesyn Embedded Technologies ausgebildetem oder im Bereich Elektronik oder Elektrotechnik qualifiziertem Personal durchgeführt werden. Die in diesem Handbuch enthaltenen Informationen dienen ausschließlich dazu, das Wissen von Fachpersonal zu ergänzen, können dieses jedoch nicht ersetzen.

Halten Sie sich von stromführenden Leitungen innerhalb des Produktes fern. Entfernen Sie auf keinen Fall Abdeckungen am Produkt. Nur werksseitig zugelassenes Wartungspersonal oder anderweitig qualifiziertes Wartungspersonal darf Abdeckungen entfernen, um Komponenten zu ersetzen oder andere Anpassungen vorzunehmen.

Installieren Sie keine Ersatzteile oder führen Sie keine unerlaubten Veränderungen am Produkt durch, sonst verfällt die Garantie. Wenden Sie sich für Wartung oder Reparatur bitte an die für Sie zuständige Geschäftsstelle von Artesyn Embedded Technologies. So stellen Sie sicher, dass alle sicherheitsrelevanten Aspekte beachtet werden.

EMV

Das Produkt wurde in einem Artesyn Standardsystem getestet. Es erfüllt die für digitale Geräte der Klasse A gültigen Grenzwerte in einem solchen System gemäß den FCC-Richtlinien Abschnitt 15 bzw. EN 55022 Klasse B. Diese Grenzwerte sollen einen angemessenen Schutz vor Störstrahlung beim Betrieb des Produktes in Gewerbe- sowie Industriegebieten gewährleisten.

Das Produkt arbeitet im Hochfrequenzbereich und erzeugt Störstrahlung. Bei unsachgemäßem Einbau und anderem als in diesem Handbuch beschriebenen Betrieb können Störungen im Hochfrequenzbereich auftreten.

Wird das Produkt in einem Wohngebiet betrieben, so kann dies mit grosser Wahrscheinlichkeit zu starken Störungen führen, welche dann auf Kosten des Produktanwenders beseitigt werden müssen. Änderungen oder Modifikationen am Produkt, welche ohne ausdrückliche Genehmigung von Artesyn Embedded Technologies durchgeführt werden, können dazu führen, dass der Anwender die Genehmigung zum Betrieb des Produktes verliert. Boardprodukte werden in einem repräsentativen System getestet, um zu zeigen, dass das Board den oben aufgeführten EMV-Richtlinien entspricht. Eine ordnungsgemässe Installation in einem System, welches die EMV-Richtlinien erfüllt, stellt sicher, dass das Produkt gemäss den EMV-Richtlinien betrieben wird. Verwenden Sie nur abgeschirmte Kabel zum Anschluss von Zusatzmodulen. So ist sichergestellt, dass sich die Aussendung von Hochfrequenzstrahlung im Rahmen der erlaubten Grenzwerte bewegt.

Warnung! Dies ist eine Einrichtung der Klasse A. Diese Einrichtung kann im Wohnbereich Funkstörungen verursachen. In diesem Fall kann vom Betreiber verlangt werden, angemessene Maßnahmen durchzuführen.

Betrieb

1 Beschädigung des Produktes
Hohe Luftfeuchtigkeit und Kondensat auf der Oberfläche des Produktes können zu Kurzschlüssen führen.
Betreiben Sie das Produkt nur innerhalb der angegebenen Grenzwerte für die relative Luftfeuchtigkeit und Temperatur. Stellen Sie vor dem Einschalten des Stroms sicher, dass sich auf dem Produkt kein Kondensat befindet.

Beschädigung von Schaltkreisen
Elektrostatische Entladung und unsachgemäßer Ein- und Ausbau des Produktes kann Schaltkreise beschädigen oder ihre Lebensdauer verkürzen.
Bevor Sie das Produkt oder elektronische Komponenten berühren, vergewissern Sie sich, daß Sie in einem ESD-geschützten Bereich arbeiten.

Fehlfunktion des Produktes
Schalter, die mit 'Reserved' gekennzeichnet sind, können mit produktionsrelevanten Funktionen belegt sein. Das Ändern dieser Schalter kann im normalen Betrieb Störungen auslösen.
Verstellen Sie nur solche Schalter, die nicht mit 'Reserved' gekennzeichnet sind. Prüfen und ggf. ändern Sie die Einstellungen der nicht mit 'Reserved' gekennzeichneten Schalter, bevor Sie das Produkt installieren.

Installation

Datenverlust
Das Herunterfahren oder die Deinstallation eines Boards bevor das Betriebssystem oder andere auf dem Board laufende Software ordnungsmemäss beendet wurde, kann zu partiellem Datenverlust sowie zu Schäden am Filesystem führen.
Stellen Sie sicher, dass sämtliche Software auf dem Board ordnungsgemäss beendet wurde, bevor Sie das Board herunterfahren oder das Board aus dem Chassis entfernen.

Beschädigung des Produktes
Fehlerhafte Installation des Produktes kann zu einer Beschädigung des Produktes führen.
Verwenden Sie die Handles, um das Produkt zu installieren/deinstallieren. Auf diese Weise vermeiden Sie, dass das Face Plate oder die Platine deformiert oder zerstört wird.

Beschädigung des Produktes und von Zusatzmodulen
Fehlerhafte Installation von Zusatzmodulen, kann zur Beschädigung des Produktes und der Zusatzmodule führen.
Lesen Sie daher vor der Installation von Zusatzmodulen die zugehörige Dokumentation.

Kabel und Stecker

Beschädigung des Produktes
Bei den RJ-45-Steckern, die sich an dem Produkt befinden, handelt es sich entweder um Twisted-Pair-Ethernet (TPE) oder um E1/T1/J1-Stecker. Beachten Sie, dass ein versehentliches Anschließen einer E1/T1/J1-Leitung an einen TPE-Stecker das Produkt zerstören kann.

- Kennzeichnen Sie deshalb TPE-Anschlüsse in der Nähe Ihres Arbeitsplatzes deutlich als Netzwerkanschlüsse.
- Stellen Sie sicher, dass die Länge eines mit Ihrem Produkt verbundenen TPE-Kabels 100 m nicht überschreitet.
- Das Produkt darf über die TPE-Stecker nur mit einem Sicherheits-Kleinspannungs-Stromkreis (SELV) verbunden werden.

Bei Fragen wenden Sie sich an Ihren Systemverwalter.

Batterie

Beschädigung des Blades

Ein unsachgemäßer Einbau der Batterie kann gefährliche Explosionen und

Beschädigungen des Blades zur Folge haben.

Verwenden Sie deshalb nur den Batterietyp, der auch bereits eingesetzt wurde und

befolgen Sie die Installationsanleitung.

Datenverlust
Wenn Sie die Batterie austauschen, können die Zeiteinstellungen verloren gehen. Eine Backupversorgung verhindert den Datenverlust während des Austauschs.
Wenn Sie die Batterie schnell austauschen, bleiben die Zeiteinstellungen möglicherweise erhalten.

Datenverlust
Wenn die Batterie wenig oder unzureichend mit Spannung versorgt wird, wird der RTC initialisiert.
Tauschen Sie die Batterie aus, bevor sieben Jahre tatsächlicher Nutzung vergangen sind.

Schäden an der Platine oder dem Batteriehalter
Wenn Sie die Batterie mit einem Schraubendreher entfernen, können die Platine oder der Batteriehalter beschädigt werden.
Um Schäden zu vermeiden, sollten Sie keinen Schraubendreher zum Ausbau der Batterie verwenden.

Umweltschutz

Entsorgen Sie alte Batterien und/oder Blades/Systemkomponenten/RTMs stets gemäß der in Ihrem Land gültigen Gesetzgebung, wenn möglich immer umweltfreundlich.